Wave Generator Xpress

Data sheet

! READ THIS FIRST !

This revision of Wave Generator Data Sheet is valid for devices sold from September 2011.

Please check your unit 'hardware revision'. The 'hardware revision' is composed of the 2 first digits of your unit's serial number, and is located on a label at the back of your device. It should be 01, 02 or 03 or higher.

This document is valid for hardware revision 03 and higher.

For older devices (HW rev 01 or 02), please refer to revision 1.01 of this data sheet, available from: http://www.byteparadigm.com/documentation-15.html

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References

[1]   8PI Control Panel User's Guide (ug_8PIControlPanel.doc)

[2]   TCL scripting for ADWG application (ug _ADWGTclLib.pdf)
      This document explain how to use the ADWG mode of operation using the Tcl scripting interface. It
      also contains a complete list of all available procedures to operate in ADWG mode.

[3]   C/C++ library for ADWG application (ug_ADWGCLib.pdf)
      This document describes how to use the C/C++ library provided with the ADWG application.

Revision history

Version	Date	Description
1.00	March 2008	First release
1.01	August 2009	Added HW revision changes
1.02	August 2011	Modification for memory / speed upgrade This data sheet is valid for Wave Generator Xpress devices sold from September 2011 For older devices, please refer to version 1.01 of this data sheet, available on: http://www.byteparadigm.com/documentation-15.html
1.03	February 2012	Minor corrections
1.04	May 2012	Updated I/O voltage specs and added minor corrections
1.05	February 2015	Updated frequency specification in case an external clock is used

This document can be updated without prior notice.

Wave Generator Xpress

Data sheet

1 Features

▸ High-speed USB 2.0 host interface (full-speed 12 Mbps and high-speed 480 Mbps)
▸ 16 output data lines for digital pattern generation
▸ 8 MB internal memory buffer
▸ 100 MHz maximum frequency on all signals
▸ 6 control lines for in/out clocking, triggering and repetitive sequence generation
▸ Maximum burst throughput: 200 MByte/s
▸ Indicative actual sustainable continuous throughput: 11 MByte/s[1]
▸ Up to 100 MByte and 100 MSample total data depth per run
▸ Selectable internal (USB bus) or external power supply for I/Os voltages
▸ I/O voltage from 1.25V to 3.3V
▸ Delivered with the 8PI Control Panel software suite, ADWG mode of operation license included
▸ Applications:
  o ASIC, FPGA, DAC and digital board verification / characterisation;
  o Automated stimulus generation;
  o Data source emulation
  o Bus master emulation;
  o System debug and system prototype access;
  o IP evaluation;

2 Wave Generator Xpress Overview

Byte Paradigm Wave Generator Xpress (or Wave Gen Xpress / WG Xpress) is a USB 2.0 high speed digital pattern generator or arbitrary digital waveform generator. It generates arbitrary digital stimuli on up to 16 bits, 100 MByte and 100 MSample data depth per run, at up to 100 MSample/s.

It is typically used to send arbitrary stimuli to your board or chip prototype, exercise custom digital interfaces and produce arbitrary digital sample streams to your system under test. Wave Generator Xpress is a convenient, robust and compact personal pattern generator for a wide variety of test and debug tasks on electronic systems.
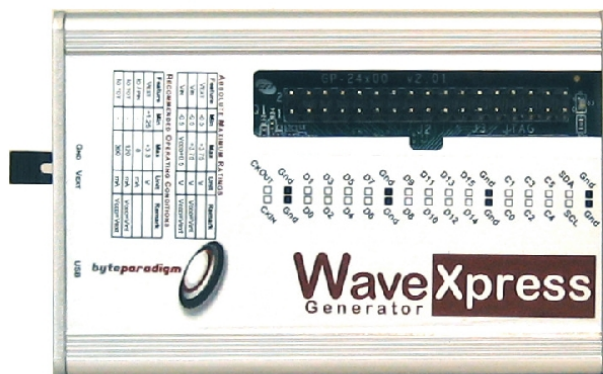
Figure 1:   Wave Generator Xpress

Wave Generator Xpress is controlled with the 8PI Control Panel Software freely licensed with the ADWG (Arbitrary Digital Waveform Generator) mode of operation. With its multiple graphical and programming (TCL/tk and C/C++) interfaces, you have many flexible options to generate stimuli, from binary or text file to whole algorithms programmed in Tcl/tk, C/C++, Visual Basic and many others.

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[1] Informative only – depends on the host PC.

3 Connecting the Wave Generator Xpress

3.1 Wave Generator Xpress at a glance

Figure 2: Wave Generator Xpress overview
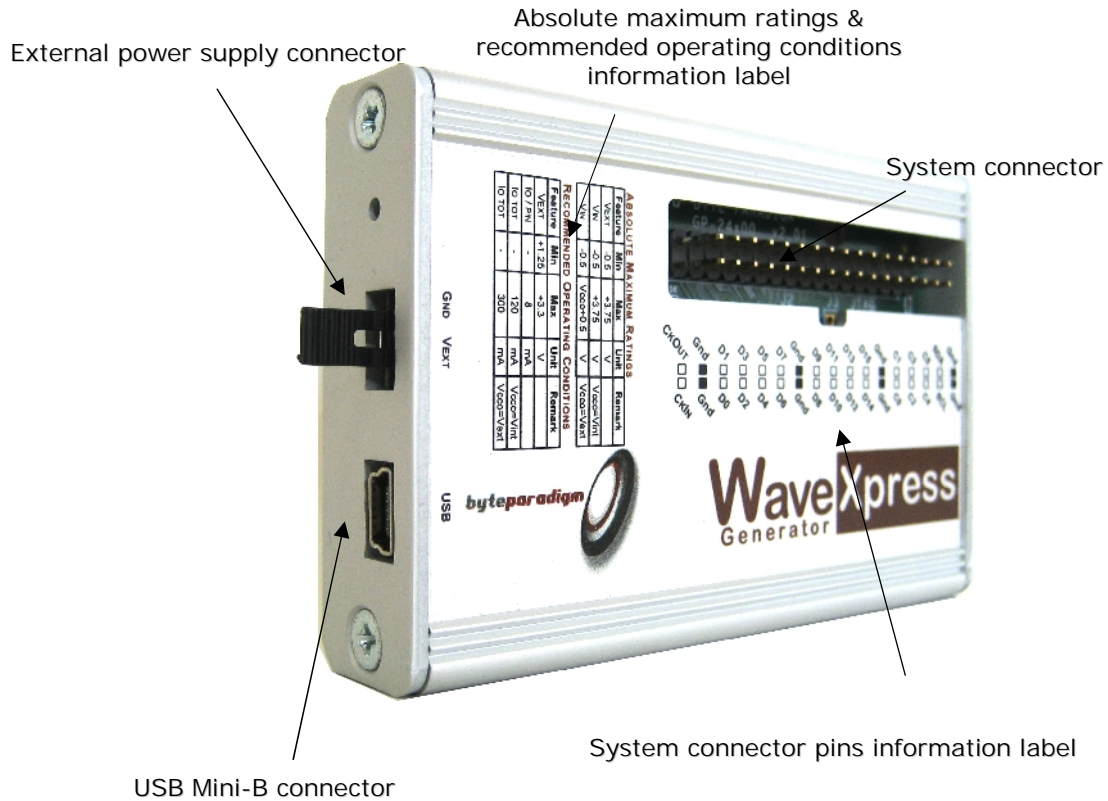
3.2 Minimum Host PC requirements

Wave Generator Xpress connects to any PC using Microsoft Windows XP / 7 (32 bit / 64 bit) operating systems through a USB 2.0 port connector.

3.3 Operating power

The main power supply of the Wave Generator Xpress is taken from the USB bus to provide the necessary voltage to the device core. The system interface can be powered either from the USB bus (internal power supply mode), either from an external power supply.

When the internal power supply mode is selected, the Wave Generator Xpress is then fully bus powered and operates without any external power supply. In this mode, the voltage level of the system interface is fixed to +3.3V (Refer to section "5 DC and Switching Characteristics" for more details on the compatible I/O voltage levels for the system connector).

The system connector can however operate at different voltage level between +1.25V and +3.3V. To enable this mode, an external power supply must be applied to the system connector V_{EXT} pins and the external supply mode must be selected.

Several hardware revisions of the Wave Generator Xpress exist. Please first check the serial number located at the back of the device, with a barcode. The 2 first digits are the hardware revision number. It can be 01, 02 or 03. According to the hardware revision, the device features are slightly different.

For devices with hardware revision 01 or 02, please check version 1.01 of this data sheet available on: http://www.byteparadigm.com/documentation-15.html.

For Hardware revision starting with 03 or higher

An external power supply connector is located at the side of the device. It is protected with a jumper. This power connector is labelled "GND VEXT". ! Respect the connector polarity when using !

Figure 3:   System connector external power supply pins for HW revision 03

VEXT connector location
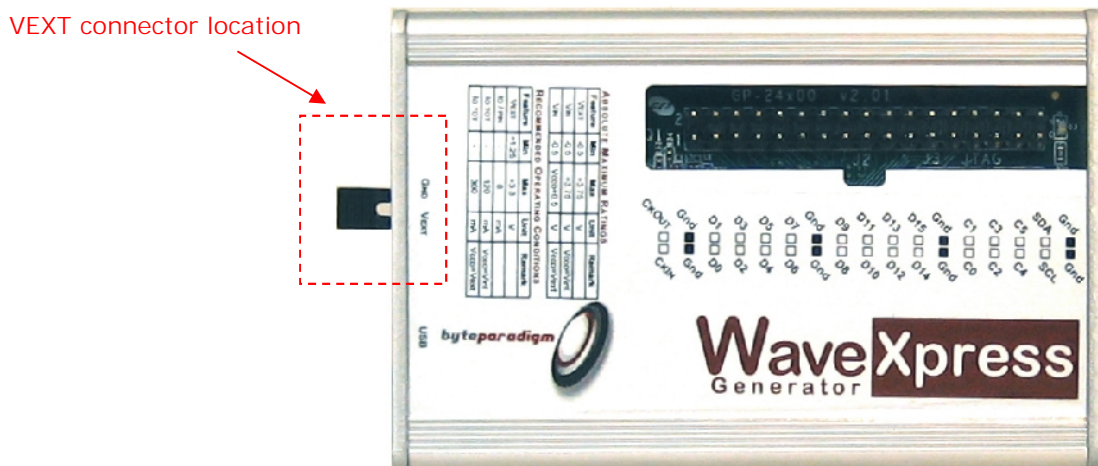
Figure 4:   USB mini-B to USB type A cable

Enabling the external power mode:
1.   Disconnect the device from the USB bus
2.   Remove the jumper from the VEXT connector
3.   Connect and apply the external power supply to the V_{EXT} pins of the system connector.
4.   Connect the device to the USB bus.
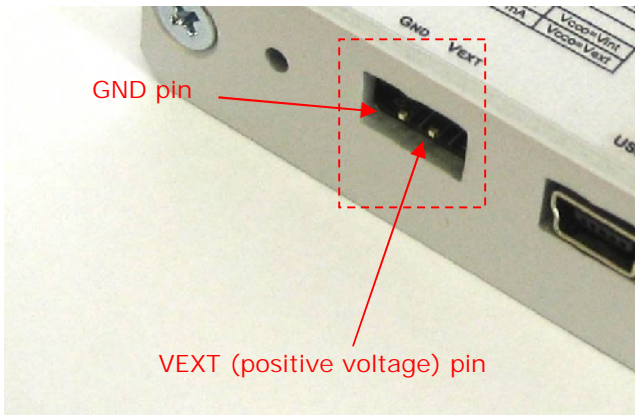5.   Once 8PI Control Panel is started, you can select the chosen voltage from Tools>Select Device and I/O Voltage drop down menu. This additional selection configures the device I/Os with signal electrical characteristics that match the supplied external voltage.
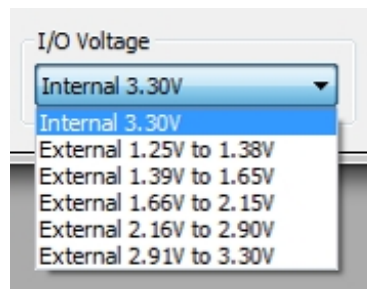
Enabling the internal power mode (bus powered):
1.   Disconnect the device from the USB bus
2.   Shut down and disconnect the external power supply.
3.   Connect the device to the USB bus.

3.4 USB and system interface connections

A 2 meters USB mini-B to USB type A is provided with all Wave Generator Xpress packages (Figure 4).

A set of 34 flying lead wires connect the Wave Generator Xpress to the board under test. A standard pin header with 2.54 mm (0.1 inch) pitch must be foreseen on the target board where access is desired. A standard 34 way F-F flat cable (delivered as option) can also be used but offers less flexibility for pin mapping and for the connection of multiple board access points.

4 Wave Generator Xpress functional description

4.1 Flexible system interface

Features:

- Up to 16 data lines and 6 control lines;
- Individual functional signal allocation onto the system connector;
- Internal or external clocking reference - 1 specific control input for external clocking;

4.1.1 Data / Control partition, allocation and configuration

The system interface connects the Wave Generator Xpress to the electronic system under test. For that purpose, a set of flying leads wires ensure the link between the system under test and the Wave Generator Xpress system connector. Using flying leads wires offer a 'physical flexibility' for Wave Generator Xpress / system signal mapping.

As depicted on the figure below, the system connector pins are grouped as data pins and control pins. The SDA and SCL pins are unused for Wave Gen Xpress.

For hardware revision 03 or higher

Figure 5: System connector pin groups allocation for HW revision 03
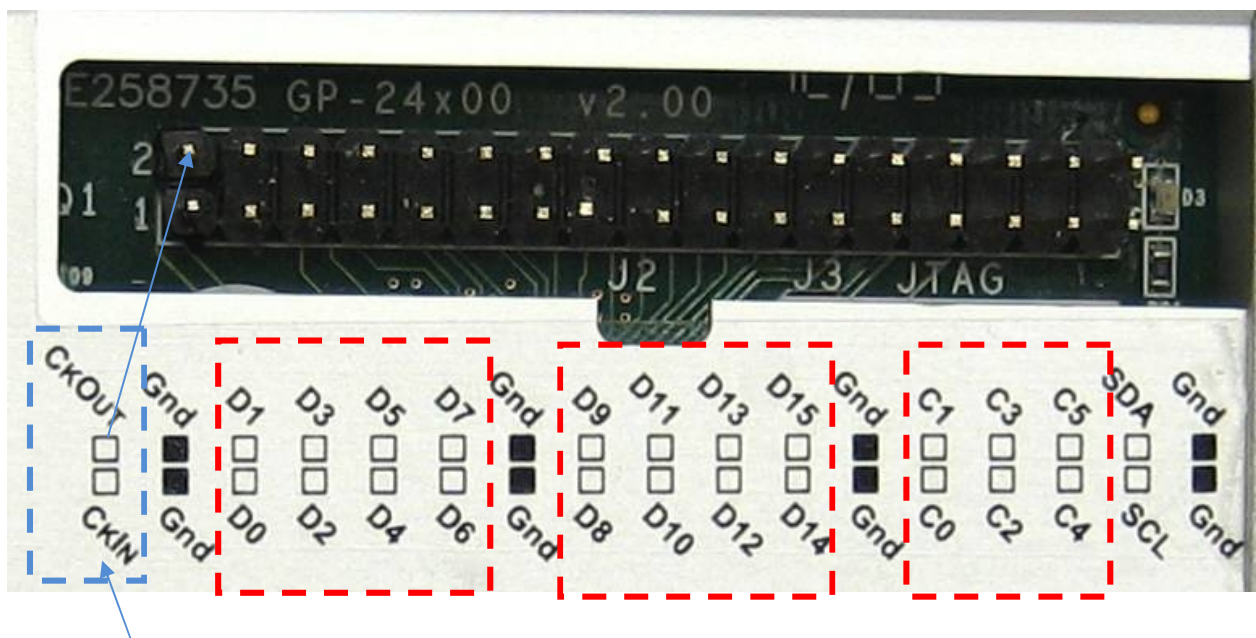
Dedicated clk in/out pins

Wave Generator Xpress I/O connector pins are grouped as 'data signals' or 'control signals'. See Table 1 for details.

Table 1: Control / Data signals definition

Signal type	Direction	Description / Usage
Control	Output	The user can define one or several repetitive output control sequences managed autonomously by the Wave Generator Xpress Accelerator. For example, output control sequences are used for repetitive signal sequences for which timing is critical.
Control	Input	The user can define one or several input control sequences used as event to trigger an autonomous response from the Wave Generator Xpress. The history of the inputs on the control lines cannot be collected by the host computer through the USB 2.0 connection. For example, input control sequences are used as start trigger to collect data (on the data pins) and send them to the host computer.
Data	Output	The data sent to the Wave Generator Xpress system connector are defined and updated by the user through the host software. Repetitive sets of data can be defined as well and memorised in the Wave Generator Xpress Accelerator embedded memory.

4.1.2   System interface clocks

Two optional clock signals can be mapped onto the system connector:
- ▸ An input clock signal: this clock signal comes from the system under test and is used as the reference clock signal to generate and sample data and controls onto the system connector. If this clock signal is used, it must be mapped onto:
  - o the system connector D20 control pin if the hardware revision is 01;
  - o the CKIN pin if the hardware revision is 02, 03 or higher. Alternatively, if no external reference clock signal is provided, the Wave Generator Xpress internal clock signal is used.
- ▸ An output clock signal: when a clock reference has to be provided to the system under test by the Wave Generator Xpress, this signal is conventionally mapped onto:
  - o the system connector D21 pin if the hardware revision is 01;
  - o the CKOUT pin if the hardware revision is 02,03 or higher.

The Wave Generator Xpress Accelerator clock frequencies are defined through the host software. Table 2 summarises the available frequency ranges, and how to set them.

Table 2: System interface clocks frequency ranges

Clock	Frequency range	Description / Options
External reference clock	$F_{EXT} / 2^{16}$ to F_{EXT} ; F_{EXT} max = 100 MHz	
Internal reference clock	763 Hz to 100 MHz	The Wave Generator Xpress Accelerator contains a clock divider unit, programmable with a 16 bits register. If ClkDiv is the value of this register, the achieved clock frequency is: frefclk / (ClkDiv + 1)
Output clock (D21)	- to 100 MHz	

4.1.3   System interface performance

The maximum clock rate for the system connector signals is 100 MHz. When all the system interface signals are used, the maximum achievable throughput is: 16 bits x 100 MHz = 1600 Mbps, that is to say 200 MByte/s.

It is important to note that this throughput can be sustained as long as sufficient data are available. This mainly depends on the local buffering memory available for the data transfer. Up to 8 MB memory can be allocated. However, because the Wave Generator Xpress performs 'on-the-fly' data transfer from the host PC, the total data depth available is in reality limited to 100 MByte and 100 MSample, if the data transfer rate is held below a PC-dependant level. The 'sustainable continuous throughput' is an indicative figure mentioned with the Wave Generator Xpress performance figures. It is the maximum sustainable throughput for 'infinite' data transmission to and from the host PC. Tests conducted show sustainable throughput up to 11 MByte/s.

Table 3: Maximum data depth per run

Number of pins used on the connector	Maximum data depth per run (Samples)	Maximum data depth per run (Byte)
1 to 8	100 MSample	100 MByte
9 to 16	50 MSample	100 MByte

5 DC and Switching Characteristics

5.1 Absolute maximum ratings

Table 4: Absolute maximum ratings

Symbol	Description	Conditions	Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	$V_{CCO}{}^2 = V_{INT}$	-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	$V_{CCO}{}^2 = V_{EXT}$	-0.5	V_{CCO}+0.5	V

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to V_{INT} or V_{EXT} when, respectively, the internal or external supply source is selected (refer to section 3.3 for more details on the powering scheme).

5.2 Recommended operating conditions

Table 5: Recommended operating conditions

Symbol	Description		Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		+1.25[1]	+3.3	V
I_{CCO}	Quiescent supply current for any user I/O pin.		-	8	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	$V_{CCO}{}^2 = V_{INT}$	-	120	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	$V_{CCO}{}^2 = V_{EXT}$	-	300	mA
T_{OP}	Operating ambient temperature		0	45	°C
$V_{IH}{}^3$	Logic high voltage threshold	$V_{CCO}{}^2 = V_{INT}$	2.0	-	V
$V_{IL}{}^3$	Logic low voltage threshold	$V_{CCO}{}^2 = V_{INT}$	-	0.8	V

Notes:
1. This is an absolute minimum. The supply noise and accuracy must be taken into account when applying external voltage to the device. For example, if the accuracy of the supply is 5%, the provided level should be 1.25/0.95 = 1.316V.
2. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to VINT or VEXT when, respectively, the internal or external supply source is selected.
3. Refer to Figure 6 for the V_{IH} and V_{IL} threshold voltage when the external supply voltage is selected.

Figure 6:   User I/O input threshold voltage vs external supply voltage
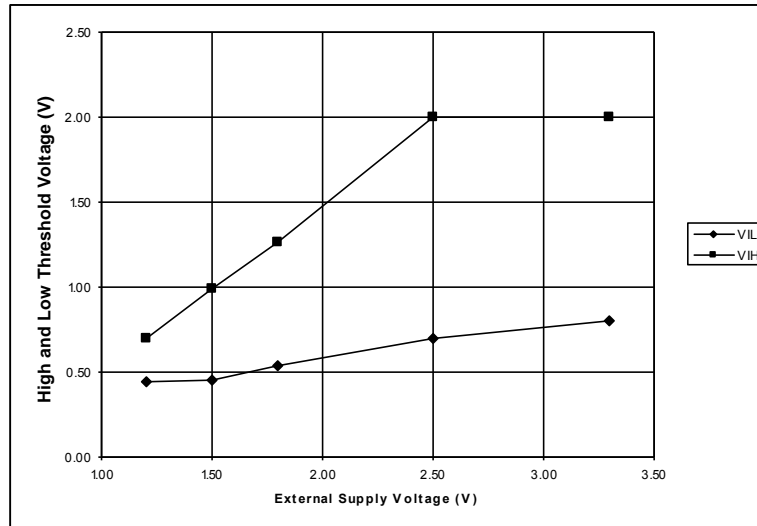
5.3 System Performance

Table 6: Data throughputs

Description	Min	Typ.	Max	Unit
USB 2.0 interface total throughput	-	-	480	Mbps
			60	MByte/s
USB 2.0 interface throughput within Wave Generator Xpress	-	-	48	MByte/s
User I/O operating frequency	-	-	100	MHz
System interface burst throughput[1]	-	-	200	MByte/s
System interface continuous throughput[2,3]	-	11	-	MByte/s

Notes:
1. The burst throughput is the performance achievable when performing transfers of 8 Mbyte or less.
2. The continuous throughput is the performance achievable when performing transfers of more than 8 Mbyte. The throughput is dependent of the host computer performances. The provided values are given as indicative reachable performance only.
3. There is no limit in the maximum amount of data that can be transferred using the Wave Generator Xpress. Continuous mode is then used to describe transfers larger than the internal device memory. The 8PI Control Panel software delivered with the Wave Generator Xpress limits a single data run to 100 MByte.

5.4 Switching Characteristics

Table 7: Clock frequencies, rise and fall time, skews

Symbol	Description	Min	Typ	Max	Unit
F_{CLKI}	Internal clock frequency	763 Hz	-	100 MHz	
F_{CLKE}	External clock frequency	2 Hz	-	100 MHz	
F_{CLKO}	Output clock frequency	-	-	100	MHz
t_{skw}[1]	Skew between clock out and the output lines when Clk$_{OUT}$ is not inverted	-400	-50	300	ps
$t_{skw,n}$[1,2]	Skew between clock out and the output lines when Clk$_{OUT}$ is inverted	T/2-400	T/2-50	T/2+300	ps
t_{lh}[3]	Output pin rise time	2.2	2.7	3.3	ns
t_{hl}[3]	Output pin fall time	4.4	5.4	6.6	ns

Notes:
1. The skew is measured taking Clk$_{OUT}$ as reference (pin P21 on the user's interface connector). It represents the offset between the reference and all the other data output pins.
2. When Clk$_{OUT}$ is inverted, the offset with the output data lines is incremented by T/2, with T equal to the output clock period.
3. Rise (10%-90%) and fall (90%-10%) time measured with internal supply voltage selected (+3.3V).

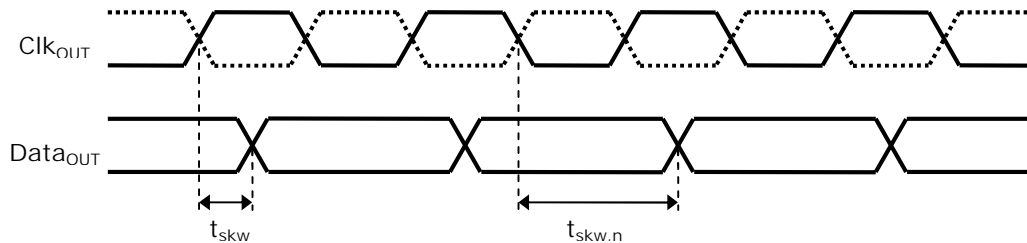Figure 7:   Skew between Clk$_{OUT}$ and data output signals, with clock ratio equal to 1

Table 8: Switching characteristics for the internal clock mode

Symbol	Description	Min	Max	Unit
$t_{co,CKout}$[1]	Clock to output delay for signal Clk$_{OUT}$	2.0	6.0	ns
$t_{co,d}$[1]	Clock to output delay for signal Clk$_{OUT}$	2.0	6.0	ns
t_{su}[2]	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho}[2]	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

Notes:
1. Values computed from used components manufacturer datasheet.
2. Setup and hold values are independent of the Clk$_{INT}$ edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.
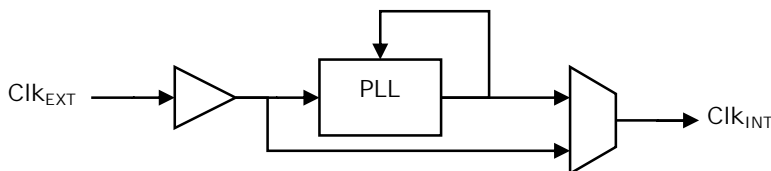
Figure 8: Switching characteristics for the internal clock
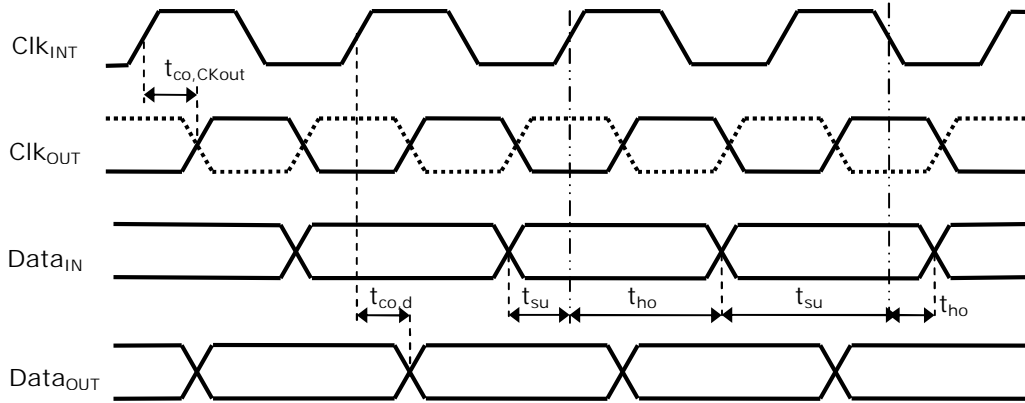
5.4.1 Using the External Clock

When the Wave Generator Xpress device operates in the external clock mode, the user supplied clock signal can follow two different clock paths to become the internal reference clock. One of the two paths includes a PLL to shorten the propagation delay. The internal clock is used as reference. All setup and hold values in this section are measured from the rising edge of to this clock Clk_{INT}.

Figure 9: Clock path from Clk_{EXT} to Clk_{INT}

When operating in arbitrary generator mode, all the outputs are generated on Clk_{INT} rising edge. Inverting the polarity of Clk_{OUT} does not change the edge used to send data out of the device.

Table 9: Switching characteristics for the external clock mode

Symbol	Description	Min	Max	Unit
$t_{co,CKout}$[3]	Clock to output delay for signal Clk_{OUT} from reference clock $Clk_{INT.}$	2.0	6.0	ns
$t_{co,d}$[3]	Clock to output delay for output data lines from reference clock Clk_{INT}	2.0	6.0	ns
t_{pce}[3]	Delay from Clk_{EXT} input pin to the internal reference clock Clk_{INT} when no PLL is inserted in the clock path.	2.7	8.4	ns
t_{pcep}[1,3]	Delay from Clk_{EXT} input pin to the internal reference clock Clk_{INT} when the PLL is inserted in the clock path.	1.8	4.5	ns
t_{su}[2]	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho}[2]	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

Notes:

1. The PLL can only be used for clock frequencies greater than or equal to 20MHz (refer to [1] for more details).
2. Setup and hold values are independent of the Clk_{INT} edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.
3. Values computed from used components manufacturer datasheet.

Figure 10:   Switching characteristics for the external clock mode