SPI Xpress

Data sheet

Revision 1.04 - July 2010

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References

[1] 8PI *Control Panel User's Guide* (ug_8PIControlPanel.pdf).

Revision history

Version	Date	Description
1.00	August 2007	Preliminary version
1.01	October 2007	First release
1.02	January 2009	Minor adaptations
1.03	August 2009	Added HW revision changes
1.04	July 2010	Some minor updates

1 Features

- High-speed USB 2.0 host interface (full-speed 12 Mbps and high-speed 480 Mbps)
- SPI 4-wires and 3-wires system interface
- Up to 50 Mbps data throughput
- Selectable internal (USB bus) or external power supply for I/Os voltages
- System interface operating from +1.8V to +3.3V
- Delivered with the 8PI Control Panel software / SPI mode of operation, including: documentation, drivers and host control software

2 SPI Xpress Overview

Byte Paradigm's SPI Xpress (Figure 1) is a high-speed SPI (Serial Peripheral Interface) master and analyser (SPI host adapter) that allows debug, analysis and testing of chips and electronic boards.

It operates on standard SPI protocol interfaces and many other serial interfaces that slightly differ from the standard SPI protocol, including 3 wires interfaces with bidirectional data line, up to 50 Mbps data rate.

SPI Xpress is delivered with 8PI Control Panel control software including the SPI application with graphical user interface, integrated waveform viewer, scripting TCL/tk interface and direct C/C++ DLL access.

Figure 1: SPI Xpress

3 Connecting the SPI Xpress device

3.1 SPI Xpress at a glance

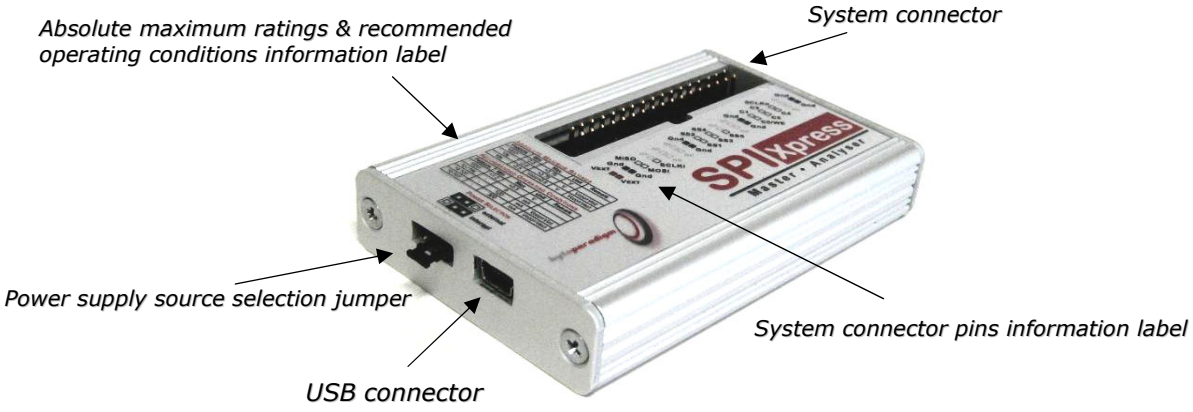


Figure 2: SPI Xpress overview

3.2 Minimum Host PC requirements

SPI Xpress connects to any PC using Microsoft Windows XP or Windows Vista operating systems through a USB 1.x or USB 2.0 port connector. For best performance, it is however recommended to use a USB 2.0 port, high-speed mode (480 Mbps).

3.3 Operating power

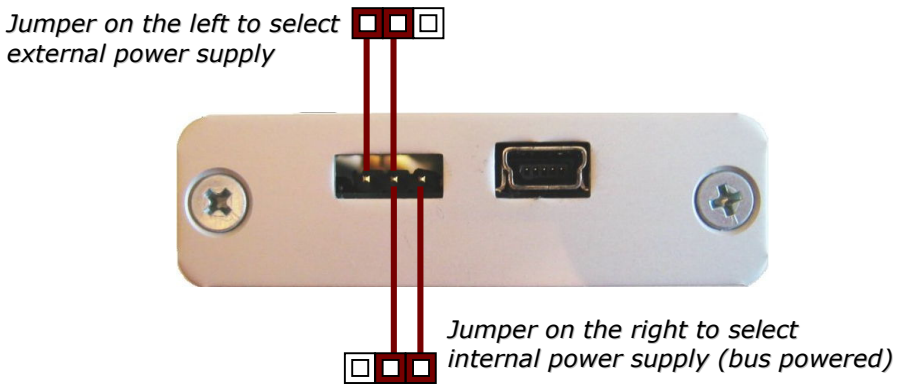
The main power supply of the SPI Xpress device is taken from the USB bus to provide the necessary voltage to the device core. The system interface can be powered either from the USB bus (internal power supply mode), either from an external power supply.
When the internal power supply mode is selected, the SPI Xpress device is then fully bus powered and operates without any external power supply. In this mode, the voltage level of the SPI interface is fixed to +3.3V (Refer to section "5 DC and Switching Characteristics" for more details on the compatible I/O voltage levels for the system connector).
The system connector can operate at different voltage level between +1.8V and +3.3V. To enable this mode, an external power supply must be applied to the system connector V_{EXT} pins and the external supply mode must be selected.

Several hardware revisions of the SPI Xpress exist. Please first check the serial number located at the back of the device, with a barcode. The 2 first digits are the hardware revision number. It can be 01, 02 or 03. According to the hardware revision, the device features are slightly different.

For Hardware revision starting with 01

A ***power supply source selection jumper*** is located at the side of the SPI XPRESS, on the left of the Mini-B USB connector. When the two left pins of the connector are shorted, the external mode is selected and an external power supply has to be provided by the user (Refer to Figure 3). When the two right pins are shorted, the internal mode is selected.

Figure 3: SPI XPRESS power source selection for HW revision 01



To switch the power supply mode the following sequences must be respected.
Enabling the external power mode:

1. Disconnect the device from the USB bus
2. Change the jumper position to select the external mode
3. Connect the system interface GND pins of the system interface to the reference of the external power supply.
4. Connect and apply the external power supply to the V_{EXT} pins of the system connector.

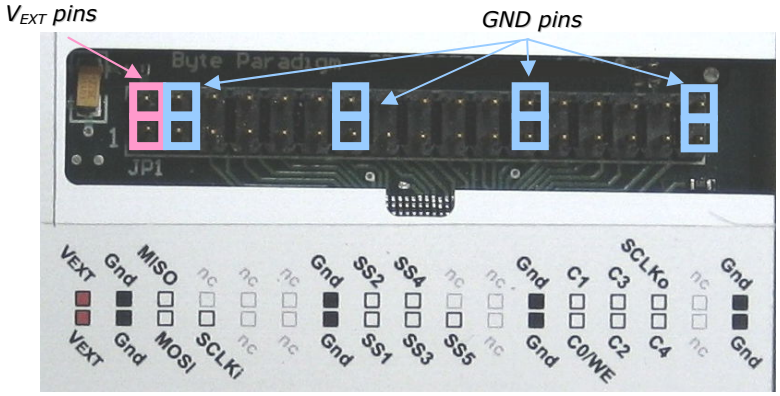
5. Connect the device to the USB bus.

Enabling the internal power mode (bus powered):

1. Disconnect the device from the USB bus
2. Shut down and disconnect the external power supply.
3. Change the jumper position to select the internal mode
4. Connect the device to the USB bus.

To improve signal integrity it is recommended to connect as many GND pins as possible to the reference ground of the system under test.

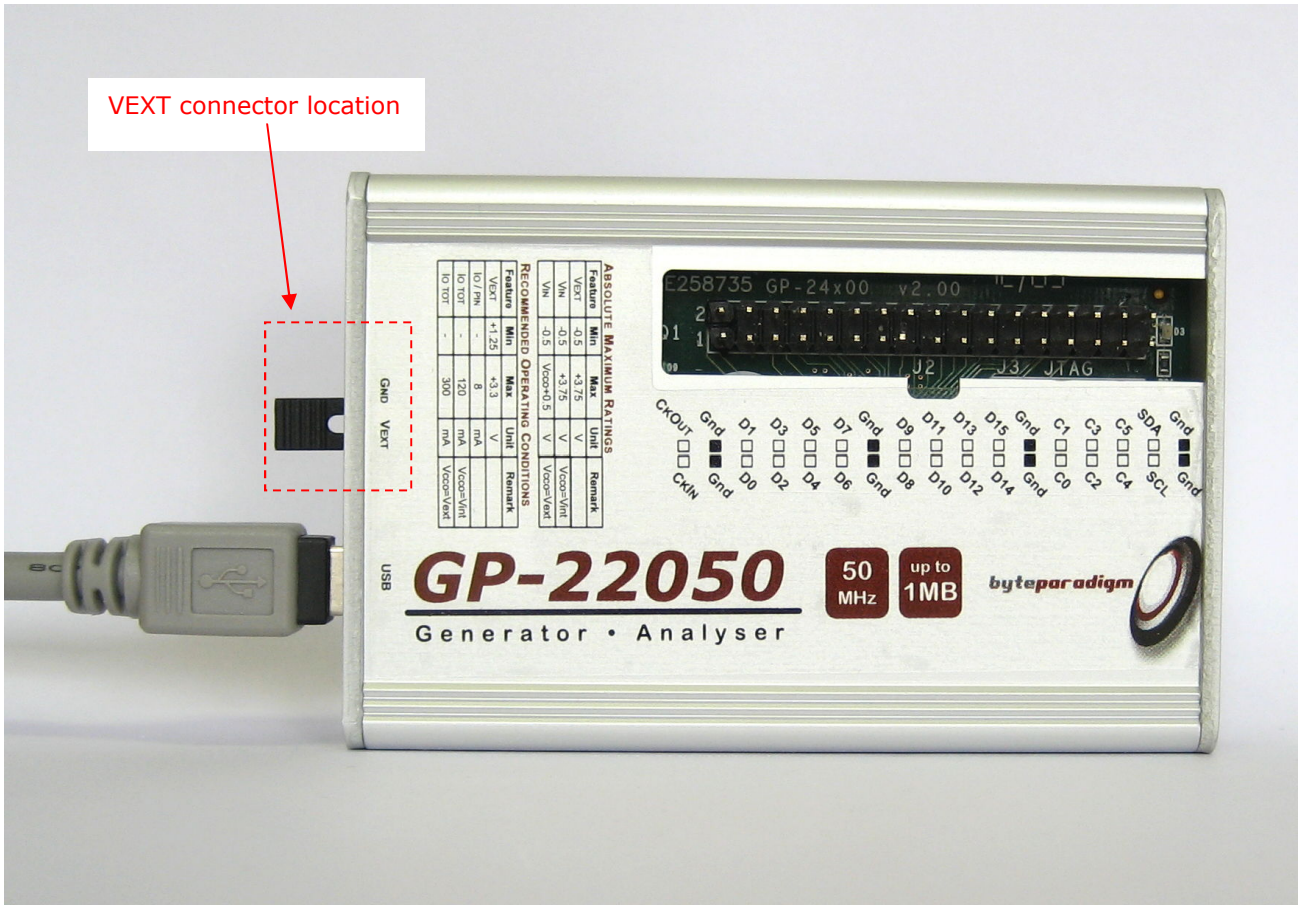
Figure 4: System connector external power supply pins for HW revision 01

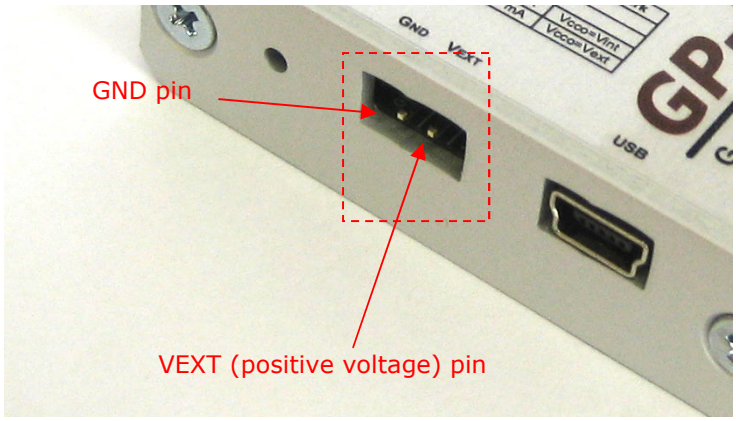


For Hardware revision starting with 02 or 03

An external power supply connector is located at the side of the device. It is protected with a jumper. This power connector is labelled "GND VEXT". **! Respect the connector polarity when using !**

Figure 5: **System connector external power supply pins for HW revision 02 or 03 (shown for GP-22050)**




GND pin
VEXT (positive voltage) pin
GND
VEXT
USB

3.4 USB and system interface connections

A 2 meters USB mini-B to USB type A is provided with the SPI Xpress device (Figure 6).

A set of 34 flying lead wires connect the SPI Xpress device to the board under test. A standard pin header with 2.54 mm (0.1 inch) pitch must be foreseen on the target board where access is desired

3.5 Hot plug and play

The SPI Xpress USB device can be attached and removed from the host computer without having to power-down or reboot. There is a delay after connecting the device to the host system before it is actually functional and reported as one of the Windows devices; during this time, the host software enables the communication with the SPI Xpress device.

Figure 6: USB mini-B to USB type A cable

4 SPI Xpress description

4.1 SPI interface

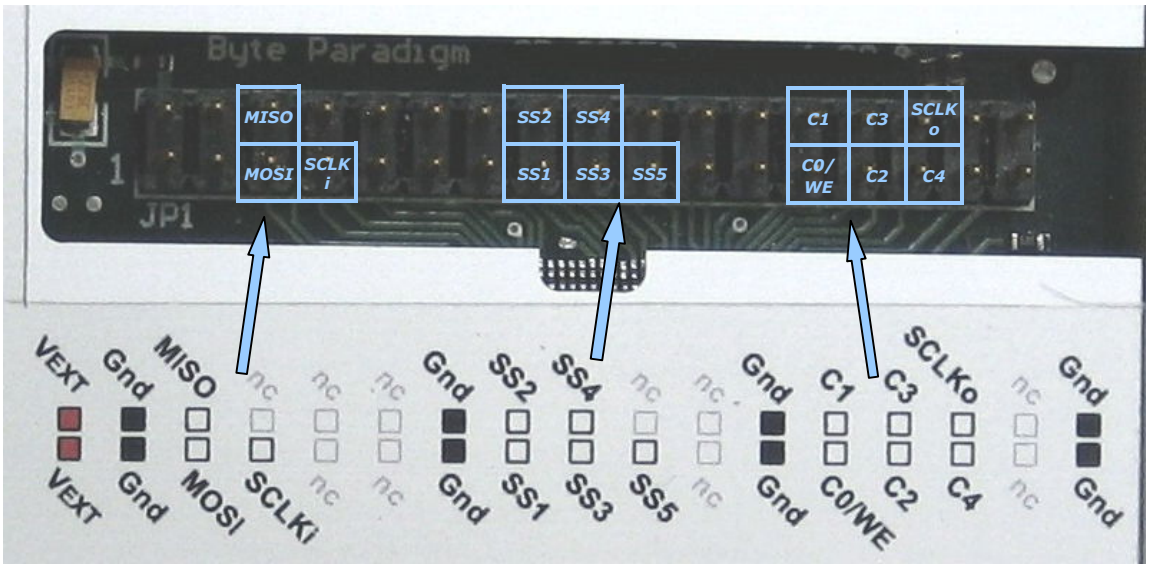
Features:

- SPI protocol master / analyser
- Supports all SPI modes
- Up to 5 slaves control
- Flexible clock generation
- SS# edge positioning
- 3-wires protocol support with bi-directional data line and optional 4th wire for bus direction
- SPI analyser with optional external trigger

4.1.1 SPI Master / Analyser pin allocation

The **SPI interface** connects the SPI Xpress device to the electronic system under test by means of a set of wires.

Figure 7: System connector pin groups allocation for HW revision 01



The pin mapping slightly differs if you use device hardware revision 02 or 03:

Figure 8: System connector pin groups allocation for HW revision 02 or 03

Besides these 2 groups, the other pins are voltage and GND pins and cannot be used for functional signalling (refer to section 3.3).

Table 1 : SPI Xpress pins

Pin name	Direction	Description / Options
V_{EXT}	-	External power supply pins – refer to section 3.3
Gnd	-	Ground pins
SPI Xpress used in master mode		
MOSI	OUT / INOUT	4-wires (SPI4) interface: MOSI (Master Out Slave In) data pin 3-wires (SPI3) interface: MOSI/MISO bi-directional data pin
MISO	IN	4-wires interface : MISO (Master In Slave Out) data pin 3-wires interface : unused
SCLKi	-	unused
SS#	OUT	SPI interface Slave select pins
C0/WE	OUT	4-wires (SPI4) interface: unused 3-wires (SPI3) interface: WE (Write Enable) pin: gives the direction of the MOSI/MISO bus. When inactive, MOSI/MISO is an input; when active, MOSI/MISO is an output
C#	-	unused
SCLKo	OUT	SPI interface SCLK: output clock pin
SPI Xpress used in analyser mode		
MOSI	IN	4-wires (SPI4) interface: MOSI (Master Out Slave In) data pin 3-wires (SPI3) interface: MOSI/MISO data pin

Pin name	Direction	Description / Options
MISO	IN	4-wires interface : MISO (Master In Slave Out) data pin 3-wires interface : unused
SCLKi	IN	SPI interface clock pin
SS#	IN	SPI interface Slave select pins
C#	IN	Control pins used as trigger inputs when the external trigger is used.
SCLKo	-	unused

4.1.2 SPI interface clocks

- When used as a **master**, the SPI Xpress device generates the SPI interface SCLK signal onto the **SCLKo** pin.
- When used as an **analyser**, the SPI Xpress samples the external analysed SPI interface clock from the **SCLKi** pin. For that sampling purpose, it uses its internal clock.

The SPI Xpress device clock frequencies are defined through the host software. Table 2 summarises the available frequency ranges, and how to set them.

Table 2: System interface clocks frequency ranges

Clock	Frequency range	Description / Options
Internal sampling clock	763 Hz to 50 MHz	The SPI Xpress device contains a clock divider unit, programmable with a 16 bits register. If ClkDiv is the value of this register, the achieved clock frequency is: frefclk / (ClkDiv + 1)
Output clock (SCLKo)	800 Hz to 50 MHz	
Input clock (SCLKi)	DC to 50 MHz	For a correct analysis of the SPI interface, the user should select the internal clock frequency with sufficient oversampling.

4.1.3 SPI interface performance

The maximum clock rate for the system connector signals is 50 MHz – hence, the maximum serial throughput is 50 Mbps.

5 DC and Switching Characteristics

5.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Description	Conditions	Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{INT}	-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{EXT}	-0.5	V_{CCO}+0.5	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to V_{INT} or V_{EXT} when, respectively, the internal or external supply source is selected (refer to section 3.3 for more details on the powering scheme).

5.2 Recommended operating conditions

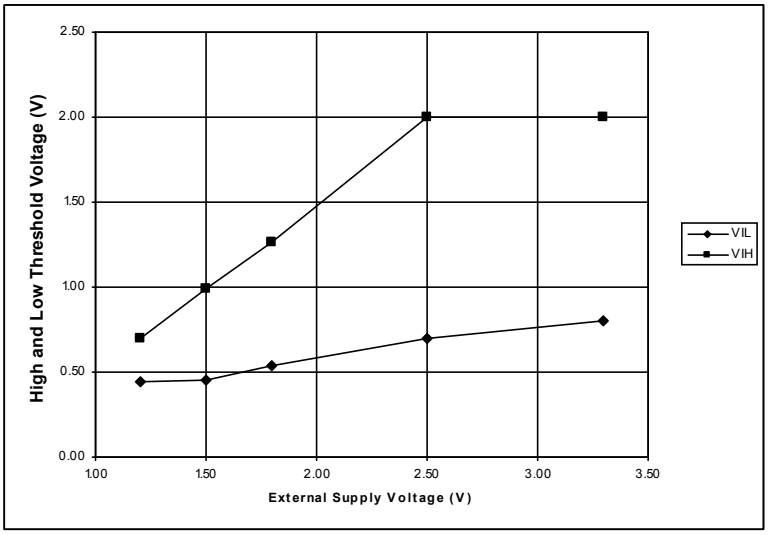
Table 4: Recommended operating conditions

Symbol	Description		Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		+1.8	+3.3	V
I_{CCO}	Quiescent supply current for any user I/O pin.		-	8	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{INT}	-	120	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{EXT}	-	300	mA
T_{OP}	Operating ambient temperature		0	45	°C
V_{IH}[2]	Logic high voltage threshold	V_{CCO}[1] = V_{INT}	2.0	-	V
V_{IL}[2]	Logic low voltage threshold	V_{CCO}[1] = V_{INT}	-	0.8	V

Notes:

1. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to VINT or VEXT when, respectively, the internal or external supply source is selected.
2. Refer to Figure 9 for the V_{IH} and V_{IL} threshold voltage when the external supply voltage is selected.

Figure 9: **User I/O input threshold voltage vs external supply voltage**



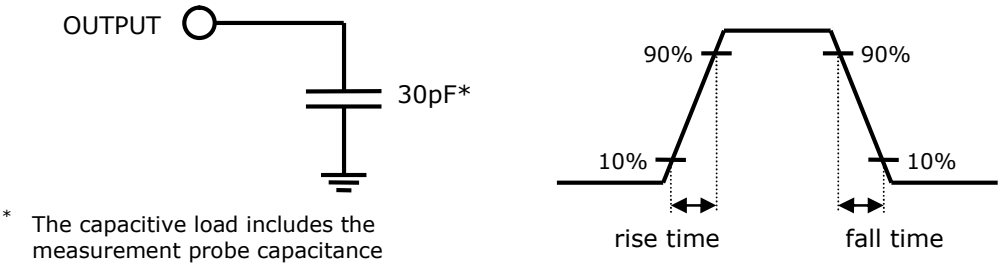
5.3 System Performance

Table 5: **Data throughputs**

Description	Min	Typ.	Max	Unit
USB 2.0 interface total throughput	-	-	480 60	Mbps MByte/s
USB 2.0 interface useful throughput for data	-	-	48	MByte/s
User I/O operating frequency	-	-	50	MHz
SPI interface burst data throughput	-	-	50	Mbit/s

5.4 Switching Characteristics

Figure 10: Tests conditions



* The capacitive load includes the measurement probe capacitance

Table 6: Clock frequencies, rise and fall time and skews

Symbol	Description	Min	Typ	Max	Unit
SCLK	SPI clock frequency	763 Hz	-	50 MHz	
t_{skw} [1]	Skew between clock out and the output lines (MOSI, SS#) when SCLK is not inverted	-400	-50	300	ps
$t_{skw,n}$ [1,2]	Skew between clock out and the output lines (MOSI, SS#) when SCLK is inverted	T/2-400	T/2-50	T/2+300	ps
t_{lh} [3]	Output pin rise time	2.2	2.7	3.3	ns
t_{hl} [3]	Output pin fall time	4.4	5.4	6.6	ns

Notes:

1. The skew is measured taking SCLK as reference (pin P21 on the user's interface connector). It represents the offset between the reference and all the other data output pins.
2. When SCLK is inverted, the offset with the output data lines is incremented by T/2, with T equal to the output clock period.
3. Rise (10%-90%) and fall (90%-10%) time measured with internal supply voltage selected (+3.3V).

Figure 11: Skew between SCLK and the output lines, with clock ratio equal to 1

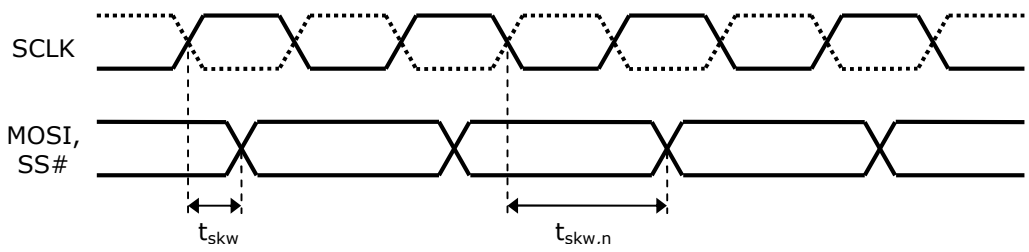


Figure 12: SPI Xpress master switching characteristics

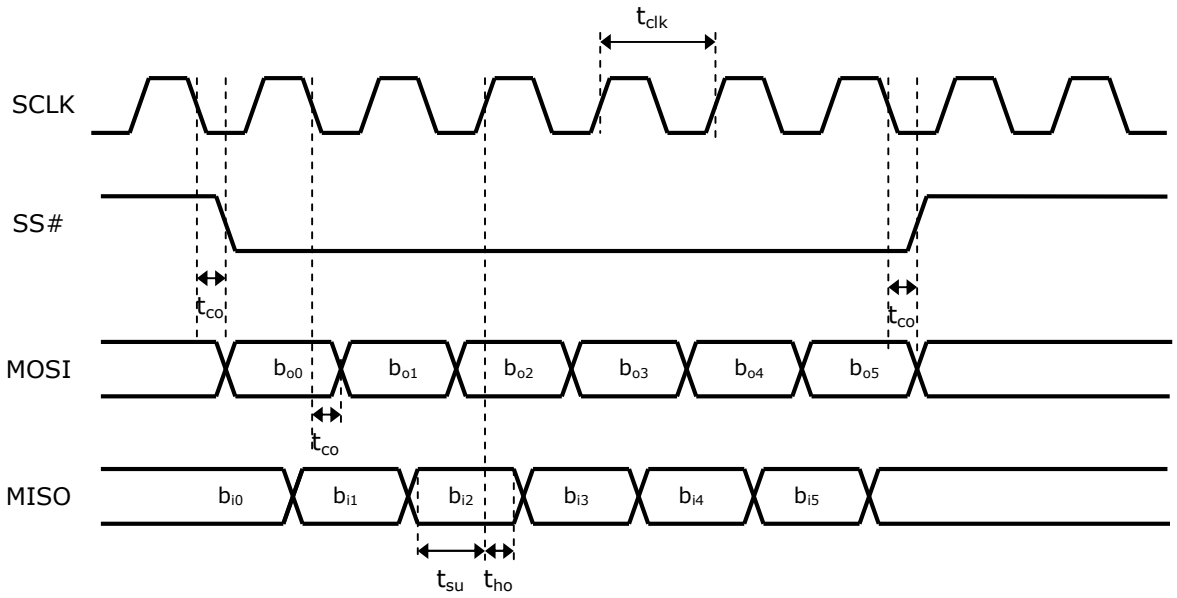


Table 7: SPI Xpress master timing parameters

Symbol	Description	Min	Typ	Max	Unit
t_{clk}	Clock period	20	-	1,250,000	ns
t_{co}	Clock to output	0	-	4	ns
t_{su}	Setup time	5.6	-	-	ns
t_{ho}	Hold time	-	-	0.0	ns