LA Xpress

Data sheet

Revision 1.00 - May 2012

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References

[1] 8PI Control Panel User's Guide (ug_8PIControlPanel.doc)

[2] TCL scripting for ADWG application (ug _AnalyserTclLib.pdf)
This document explain how to use the Analyser mode of operation using the Tcl scripting interface. It also contains a complete list of all available procedures to operate in Analyser mode.

Revision history

Version	Date	Description
1.00	May 2012	First release

1 Features

- High-speed USB 2.0 host interface
- **16 input data lines** for digital data sampling
- **8 MB** internal memory buffer
- **100 MHz** maximum sampling frequency on all signals
- 6 control lines for in/out clocking and triggering.
- Up to 100 MByte and 100 MSample total data depth per run
- Selectable internal (USB bus) or external power supply for I/Os voltages
- I/O voltage from 1.25V to 3.3V
- Delivered with the 8PI Control Panel software suite, Analyser mode of operation license included

2 LA Xpress overview

Byte Paradigm **LA Xpress** is a USB 2.0 high speed logic analyzer. It samples up to 16 bit digital data at up to 100 MSample/s. LA Xpress encloses a large **8 MByte** internal buffer.

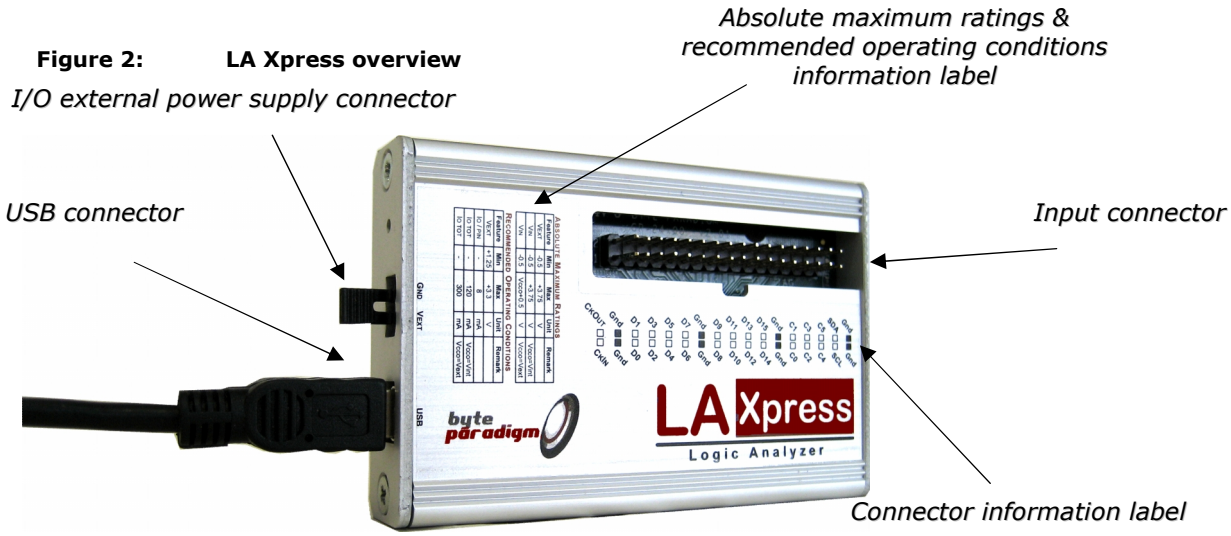
LA Xpress is controlled with the **8PI Control Panel Software** freely licensed with the **Analyser** mode of operation. With its multiple graphical and programming (C/C++ and TCL/tk) interfaces, you have many flexible options to control LA Xpress from PC.

Figure 1: LA Xpress

3 Connecting LA Xpress

3.1 LA Xpress at a glance

Figure 2: LA Xpress overview



Device dimensions (WxLxH) : 55 x 80 x 16 mm

3.2 Minimum Host PC requirements

LA Xpress connects to any PC using Microsoft Windows XP / 7 (32 bit / 64 bit) operating systems through a USB 2.0 port connector.

3.3 Operating power

The main power supply of the LA Xpress is taken from the USB bus to provide the necessary voltage to the device core. The system interface can be powered either from the USB bus (internal power supply mode), either from an external power supply.

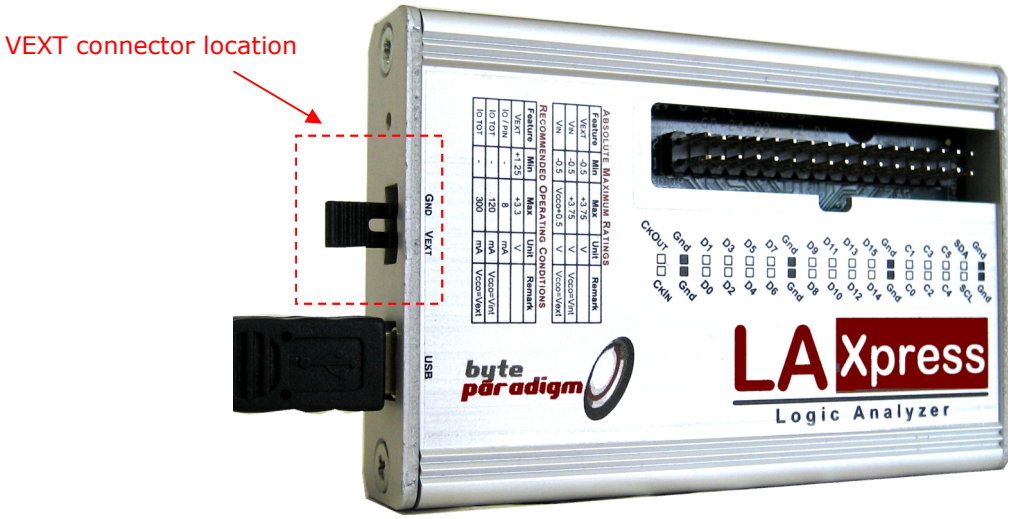
When the internal power supply mode is selected, the LA Xpress is then fully bus powered and operates without any external power supply. In this mode, the voltage level of the system interface is fixed to +3.3V (Refer to section "5 DC and Switching Characteristics" for more details on the compatible I/O voltage levels for the system connector).

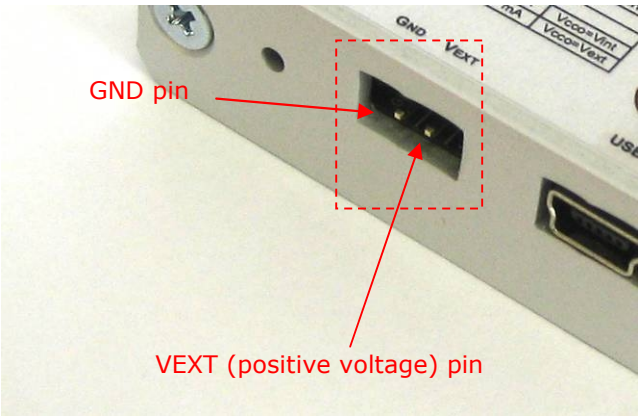
The system connector can however operate at different voltage level between +1.25V and +3.3V. To enable this mode, an external power supply must be applied to the system connector V_{EXT} pins and the external supply mode must be selected.

Several hardware revisions of the LA Xpress exist. Please first check the serial number located at the back of the device, with a barcode. The 2 first digits are the hardware revision number. It can be 04, 05 and higher... . According to the hardware revision, the device features are slightly different.

An external power supply connector is located at the side of the device. It is protected with a jumper. This power connector is labelled "GND VEXT". **! Respect the connector polarity when using !**

Figure 3: System connector external power supply





Enabling the external power mode:

1. Disconnect the device from the USB bus
2. Remove the jumper from the VEXT connector
3. Connect and apply the external power supply to the V_{EXT} pins of the system connector.
4. Connect the device to the USB bus.

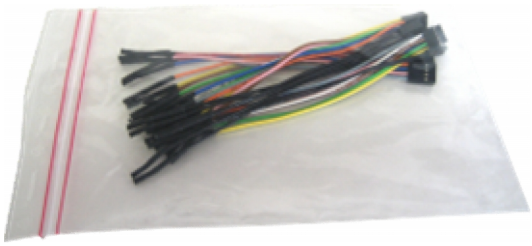
Enabling the internal power mode (bus powered):

1. Disconnect the device from the USB bus
2. Shut down and disconnect the external power supply.
3. Connect the device to the USB bus.

3.4 USB and system interface connections

A 2 meters USB mini-B to USB type A is provided with all LA Xpress packages.

A set of 34 flying lead wires connect the LA Xpress to the board under test. A standard pin header with 2.54 mm (0.1 inch) pitch must be foreseen on the target board where access is desired. A standard 34 way F-F flat cable (delivered as option) can also be used but offers less flexibility for pin mapping and for the connection of multiple board access points.



3.5 Hot plug and play

The LA Xpress USB device can be attached and removed from the host computer without having to power-down or reboot. There is a delay after connecting the device to the host system before it is actually functional and reported as one of the Windows devices; during this time, the host software detects the LA Xpress and programs its hardware settings.

4 LA Xpress functional description

4.1 Flexible system interface

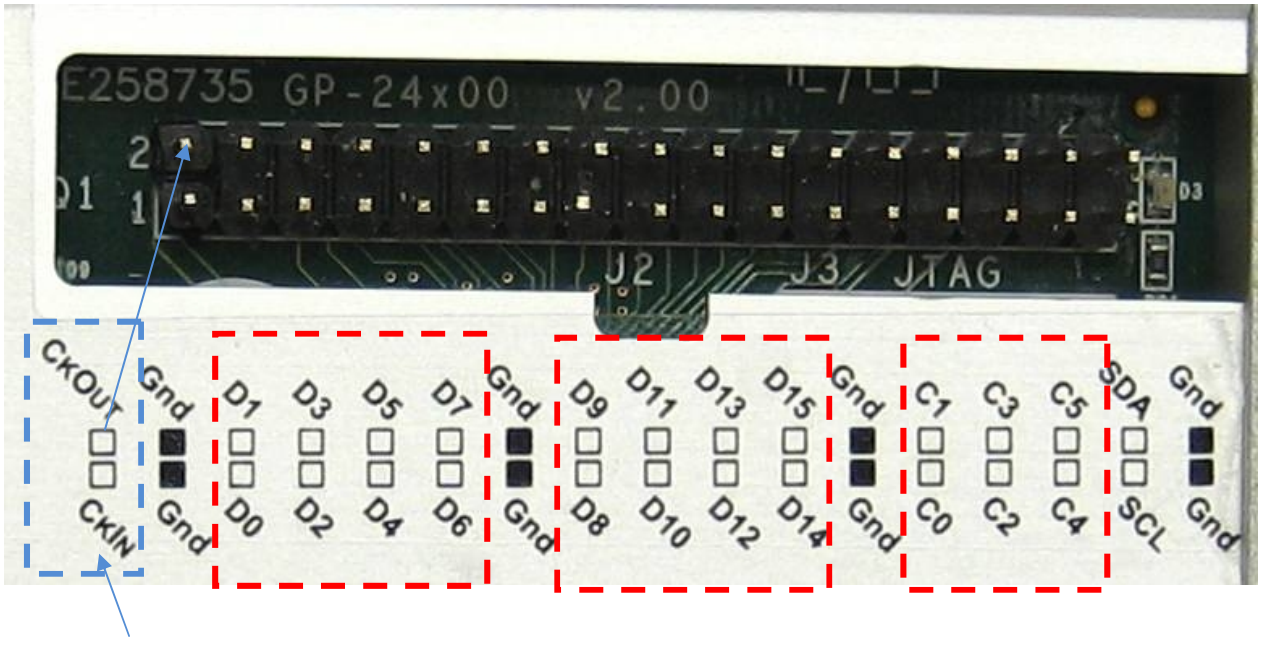
Features:

- Up to **16 data lines** and **6 control lines**;
- **Internal or external clocking reference** - 1 specific control input for external clocking;

4.1.1 Data / Control partition, allocation and configuration

The **system interface** connects the LA Xpress to the electronic system under test. For that purpose, a set of flying leads wires ensure the link between the system under test and the LA Xpress **system connector**. Using flying leads wires offer a 'physical flexibility' for LA Xpress / system signal mapping.
As depicted on the figure below, the system connector pins are grouped as **data pins** and **control pins.** The SDA and SCL pins are unused.

Figure 4: System connector pin groups allocation



Dedicated clk in/out pins

Table 1: Control / Data signals definition

Signal type	Direction	Description / Usage
Control C0...C5	Input	The user can define one or several input control sequences used as event to trigger an autonomous response from the LA Xpress. The history of the inputs on the control lines cannot be visualized onto the host computer.
Data D0...D15	Input	LA Xpress samples digital signals from this set of inputs.

For advanced use of control pins, please refer to 8PI Control Panel user's guide.

4.1.2 System interface clocks

Two optional clock signals can be mapped onto the system connector:

- An **input clock signal**: this clock signal comes from the system under test and is used as the reference clock signal to generate and sample data and controls onto the system connector. If this clock signal is used, it must be mapped onto: **CKIN pin.**
- Alternatively, if no external reference clock signal is provided, the LA Xpress internal clock signal is used.
- An **output clock signal**: when a clock reference has to be provided to the system under test by the LA Xpress, this signal is conventionally mapped onto **the CKOUT.**

The LA Xpress Accelerator clock frequencies are defined through the host software. Table 2 summarises the available frequency ranges, and how to set them.

Table 2: System interface clocks frequency ranges

Clock	Frequency range	Description / Options
External reference clock(CKIn)	F_{EXT} / 2^{16} to F_{EXT} ; F_{EXT} max = 100 MHz	
Internal reference clock	763 Hz to 100 MHz	LA Xpress contains a clock divider unit, programmable with a 16 bits register. If ClkDiv is the value of this register, the achieved clock frequency is: frefclk / (ClkDiv + 1)
Output clock (CKOut)	- to 100 MHz	

4.1.3 System interface performance

The maximum sampling rate for the system connector signals is 100 MHz. When all the system interface signals are used, the maximum achievable throughput is: 16 bits x 100 MHz = 1600 Mbps, that is to say **200 MByte/s.**

5 DC and Switching Characteristics

5.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Description	Conditions	Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{INT}	-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{EXT}	-0.5	V_{CCO}+0.5	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to V_{INT} or V_{EXT} when, respectively, the internal or external supply source is selected (refer to section 3.3 for more details on the powering scheme).

5.2 Recommended operating conditions

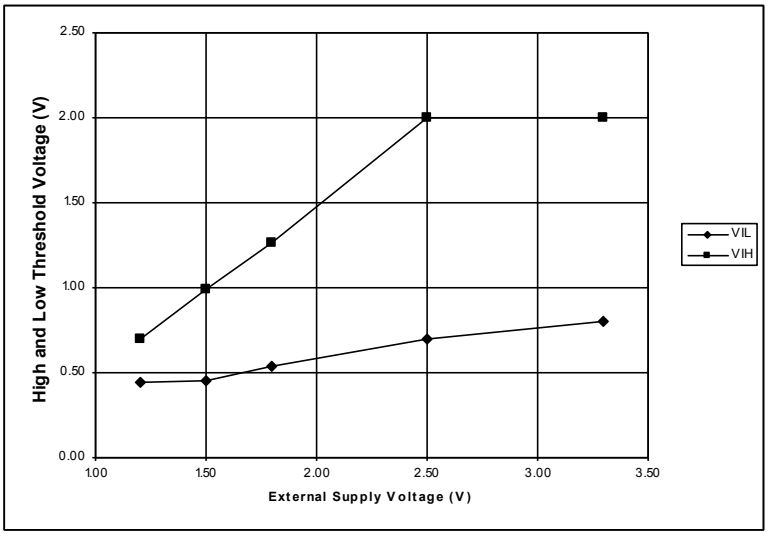
Table 4: Recommended operating conditions

Symbol	Description		Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		+1.25	+3.3	V
I_{CCO}	Quiescent supply current for any user I/O pin.		-	8	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{INT}	-	120	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{EXT}	-	300	mA
T_{OP}	Operating ambient temperature		0	45	°C
V_{IH}[2]	Logic high voltage threshold	V_{CCO}[1] = V_{INT}	2.0	-	V
V_{IL}[2]	Logic low voltage threshold	V_{CCO}[1] = V_{INT}	-	0.8	V

Notes:

1. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to VINT or VEXT when, respectively, the internal or external supply source is selected.
2. Refer to Figure 5 for the V_{IH} and V_{IL} threshold voltage when the external supply voltage is selected.

Figure 5: User I/O input threshold voltage vs external supply voltage



5.3 System Performance

Table 5: Data throughputs

Description	Min	Typ.	Max	Unit
USB 2.0 interface total throughput	-	-	480 60	Mbps MByte/s
USB 2.0 interface throughput within LA Xpress	-	-	48	MByte/s
User I/O operating frequency	-	-	100	MHz
System interface burst throughput[1]	-	-	200	MByte/s
System interface continuous throughput[2,3]	-	11	-	MByte/s

Notes:

1. The burst throughput is the performance achievable when performing transfers of 8 Mbyte or less.
2. The continuous throughput is the performance achievable when performing transfers of more than 8 Mbyte. The throughput is dependent of the host computer performances. The provided values are given as indicative reachable performance only.

5.4 Switching Characteristics

Table 6: Clock frequencies, rise and fall time, skews

Symbol	Description	Min	Typ	Max	Unit
F_{CLKI}	Internal clock frequency	763 Hz	-	100 MHz	
F_{CLKE}	External clock frequency	-	-	100	MHz
F_{CLKO}	Output clock frequency	-	-	100	MHz
t_{skw} [1]	Skew between clock out and the output lines when Clk_{OUT} is not inverted	-400	-50	300	ps
$t_{skw,n}$ [1,2]	Skew between clock out and the output lines when Clk_{OUT} is inverted	T/2-400	T/2-50	T/2+300	ps
t_{lh} [3]	Output pin rise time	2.2	2.7	3.3	ns
t_{hl} [3]	Output pin fall time	4.4	5.4	6.6	ns

Notes:

1. The skew is measured taking Clk_{OUT} as reference (pin P21 on the user's interface connector). It represents the offset between the reference and all the other data output pins.
2. When Clk_{OUT} is inverted, the offset with the output data lines is incremented by T/2, with T equal to the output clock period.
3. Rise (10%-90%) and fall (90%-10%) time measured with internal supply voltage selected (+3.3V).

Table 7: Switching characteristics for the internal clock mode

Symbol	Description	Min	Max	Unit
$t_{co,CKout}$ [1]	Clock to output delay for signal Clk_{OUT}	2.0	6.0	ns
$t_{co.d}$ [1]	Clock to output delay for signal Clk_{OUT}	2.0	6.0	ns
t_{su} [2]	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho} [2]	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

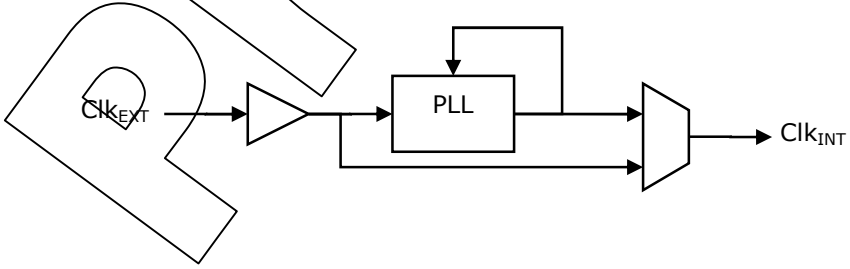
Notes:

1. Values computed from used components manufacturer datasheet.
2. Setup and hold values are independent of the Clk_{INT} edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.

5.4.1 Using the External Clock

When the LA Xpress device operates in the external clock mode, the user supplied clock signal can follow two different clock paths to become the internal reference clock. One of the two paths includes a PLL to shorten the propagation delay. The internal clock is used as reference. All setup and hold values in this section are measured from the rising edge of to this clock Clk_{INT}.

Figure 6: Clock path from Clk_{EXT} to Clk_{INT}



When operating in arbitrary generator mode, all the outputs are generated on Clk_{INT} rising edge. Inverting the polarity of Clk_{OUT} does not change the edge used to send data out of the device.

Table 8: Switching characteristics for the external clock mode

Symbol	Description	Min	Max	Unit
t_{pce} [3]	Delay from Clk_{EXT} input pin to the internal reference clock Clk_{INT} when no PLL is inserted in the clock path.	2.7	8.4	ns
t_{pcep} [1,3]	Delay from Clk_{EXT} input pin to the internal reference clock Clk_{INT} when the PLL is inserted in the clock path.	1.8	4.5	ns
t_{su} [2]	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho} [2]	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

Notes:

1. The PLL can only be used for clock frequencies greater than or equal to 20MHz (refer to [1] for more details).
2. Setup and hold values are independent of the Clk_{INT} edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.
3. Values computed from used components manufacturer datasheet.

Figure 7: Switching characteristics for the external clock mode