I²C Xpress

Data sheet

Revision 1.02 - February 2010

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References

[1] 8PI *Control Panel User's Guide* for I²C mode of operation (ug_8PIControlPanel.pdf).

Revision history

Version	Date	Description
1.00	August 2008	Preliminary version
1.01	August 2009	Added hardware revision changes
1.02	February 2010	Reviewed interface description

1 Features

- Operates on standard I²C protocol
- Low 10 Kbps, Standard 100 Kbps, Fast 400 Kbps modes support[1].
- Multi-master support
- 7 and 10 bits slave addressing support
- Repeated start support
- USB-powered, compact and robust portable solution
- Delivered with the 8PI Control Panel software / I2C mode of operation, including: documentation, drivers and host control software.

2 I²C Xpress Overview

Byte Paradigm's I²C Xpress (Figure 1) is a I²C (Serial Peripheral Interface) exerciser and analyser that allows debug, analysis and testing of chips and electronic boards.

It operates on standard I²C protocol interfaces and is ideal for master-side chip-to-chip communication emulation, I²C bus system development and debug.

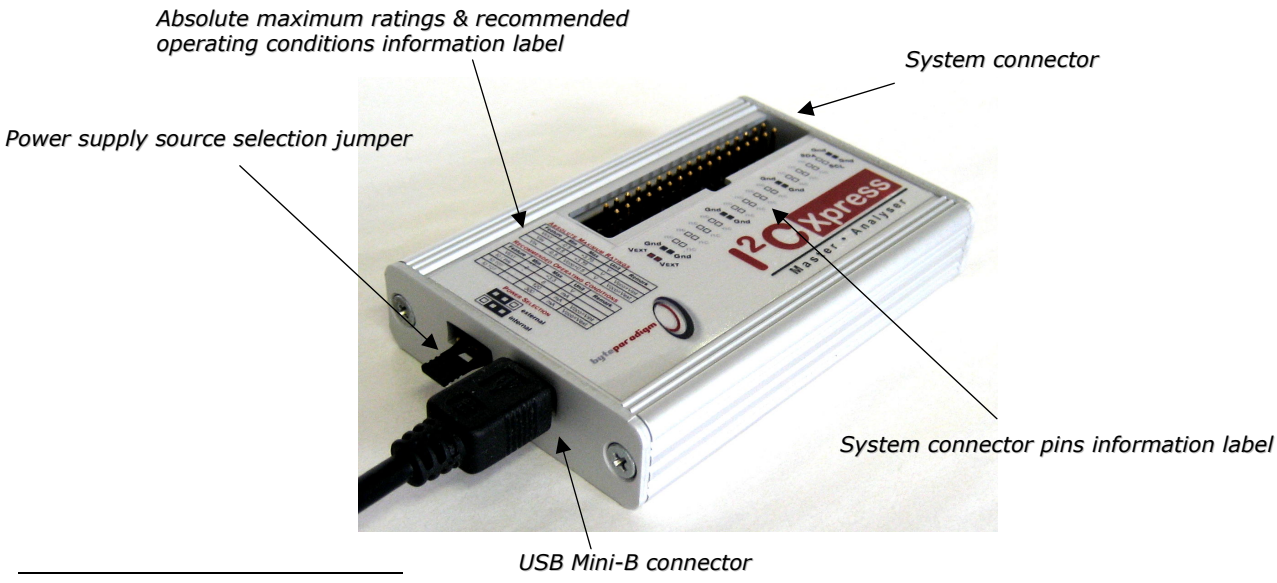
Figure 1: I²C Xpress

I²C Xpress is delivered with 8PI Control Panel control software including the I²C application with graphical user interface, integrated waveform viewer, scripting TCL/tk interface and direct C/C++ DLL access.

3 Connecting the I²C Xpress device

3.1 I²C Xpress at a glance

Figure 2: I²C Xpress overview



[1] Please contact support@byteparadigm.com for high speed 3.4 Mbps availability and support

3.2 Minimum Host PC requirements

I²C Xpress connects to any PC using Microsoft Windows XP or Windows Vista operating systems through a USB 1.x or USB 2.0 port connector. For best performance, it is however recommended to use a USB 2.0 port, high-speed mode (480 Mbps).

3.3 Operating power

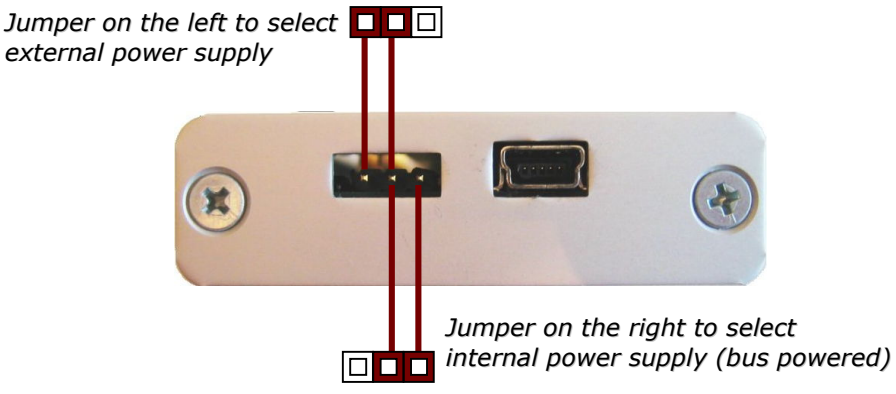
The main power supply of the I²C Xpress device is taken from the USB bus to provide the necessary voltage to the device core. The system interface can be powered either from the USB bus (internal power supply mode), either from an external power supply.
When the internal power supply mode is selected, the I²C Xpress device is then fully bus powered and operates without any external power supply. In this mode, the voltage level of the I²C interface is fixed to +3.3V (Refer to section "5 DC and Switching Characteristics" for more details on the compatible I/O voltage levels for the system connector).
The system connector can operate at a different voltage level between +1.8V and +3.3V. To enable this mode, an external power supply must be applied to the system connector V_{EXT} pins and the external supply mode must be selected.

Several hardware revisions of the SPI Xpress exist. Please first check the serial number located at the back of the device, with a barcode. The 2 first digits are the hardware revision number. It can be 01, 02 or 03. According to the hardware revision, the device features are slightly different.

For Hardware revision starting with 01

A ***power supply source selection jumper*** is located at the side of the I²C Xpress device, on the left of the Mini-B USB connector. When the two left pins of the connector are shorted, the external mode is selected and an external power supply has to be provided by the user (Refer to Figure 3). When the two right pins are shorted, the internal mode is selected.

Figure 3: I²C Xpress power source selection



To switch the power supply mode the following sequences must be respected.
Enabling the external power mode:

1. Disconnect the device from the USB bus
2. Change the jumper position to select the external mode
3. Connect the system interface GND pins of the system interface to the reference of the external power supply.
4. Connect and apply the external power supply to the V_{EXT} pins of the system connector.

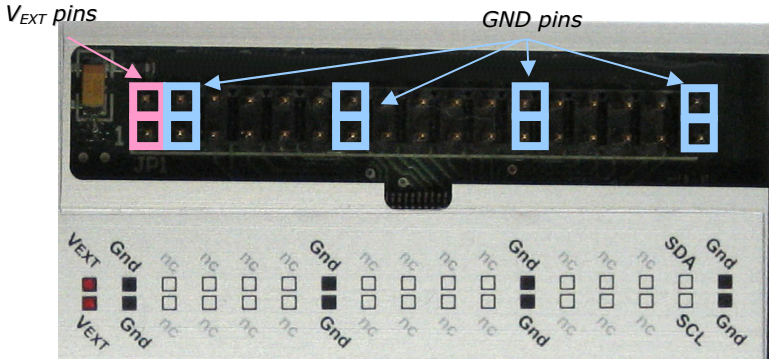
5. Connect the device to the USB bus.

Enabling the internal power mode (bus powered):

1. Disconnect the device from the USB bus
2. Shut down and disconnect the external power supply.
3. Change the jumper position to select the internal mode
4. Connect the device to the USB bus.

To improve signal integrity it is recommended to connect as many GND pins as possible to the reference ground of the system under test.

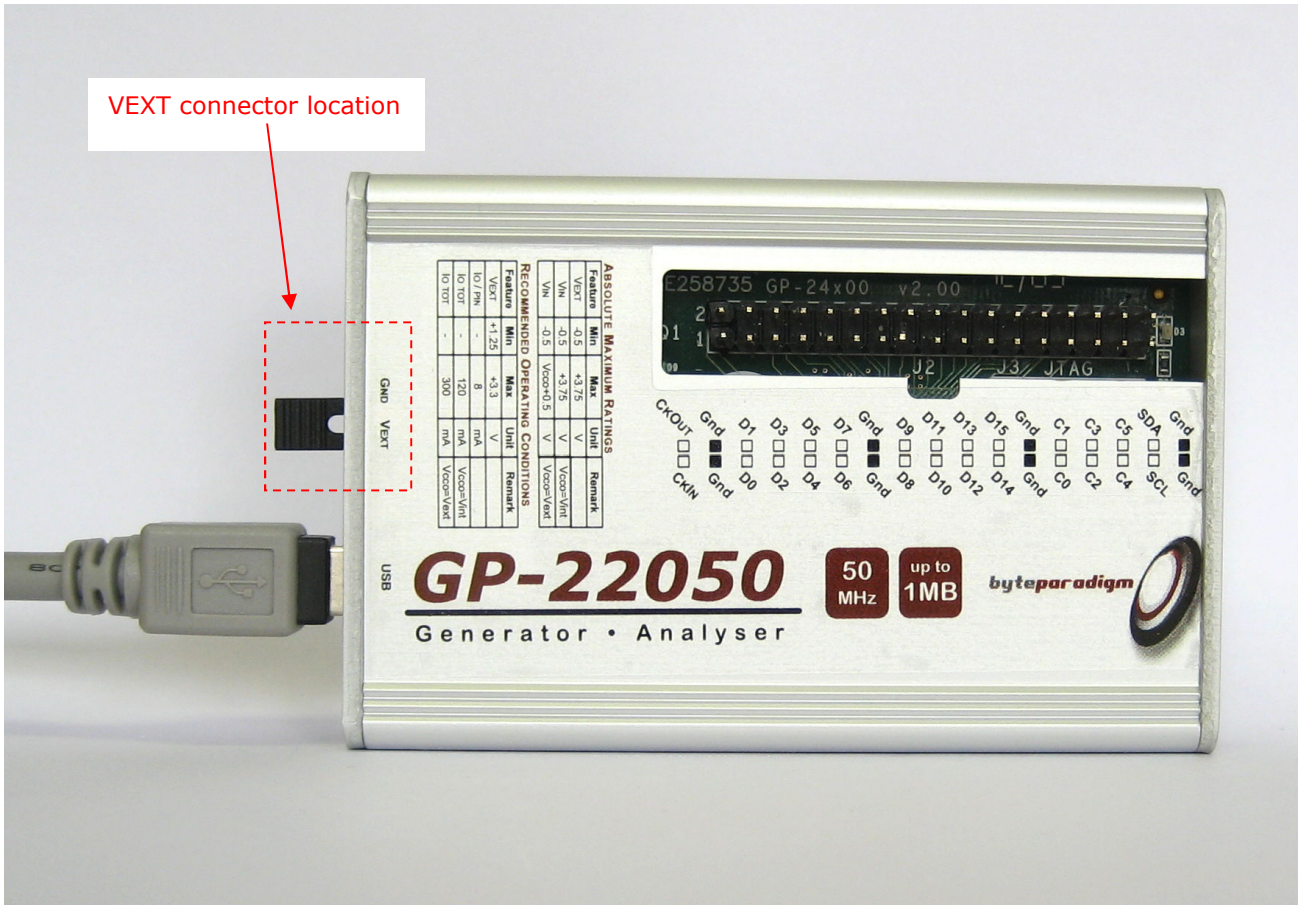
Figure 4: System connector external power supply pins

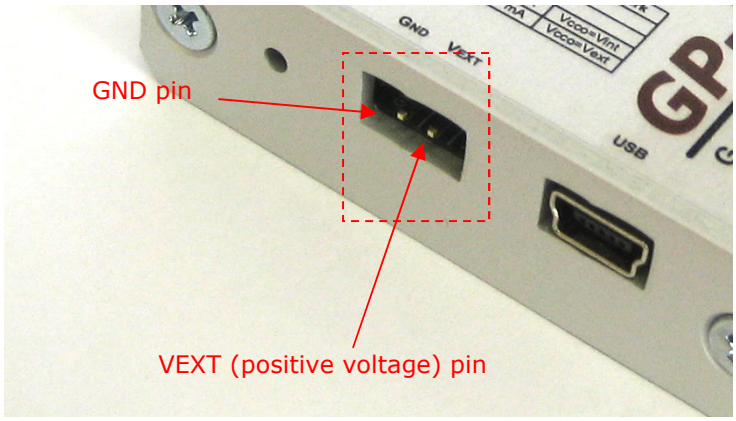


For Hardware revision starting with 02 or 03

An external power supply connector is located at the side of the device. It is protected with a jumper. This power connector is labelled "GND VEXT". **! Respect the connector polarity when using !**

Figure 5: System connector external power supply pins for HW revision 02 or 03 (shown for GP-22050)





3.4 USB and system interface connections

A 2 meters USB mini-B to USB type A is provided with the I²C Xpress device (Figure 6).

A set of 34 flying lead wires connect the I²C Xpress device to the board under test. A standard pin header with 2.54 mm (0.1 inch) pitch must be foreseen on the target board where access is desired

3.5 Hot plug and play

The I²C Xpress USB device can be attached and removed from the host computer without having to power-down or reboot. There is a delay after connecting the device to the host system before it is actually functional and reported as one of the Windows devices; during this time, the host software enables the communication with the I²C Xpress device.

Figure 6: USB mini-B to USB type A cable

4 I²C Xpress description

4.1 I²C interface

4.1.1 I²C Master / Analyser pin allocation

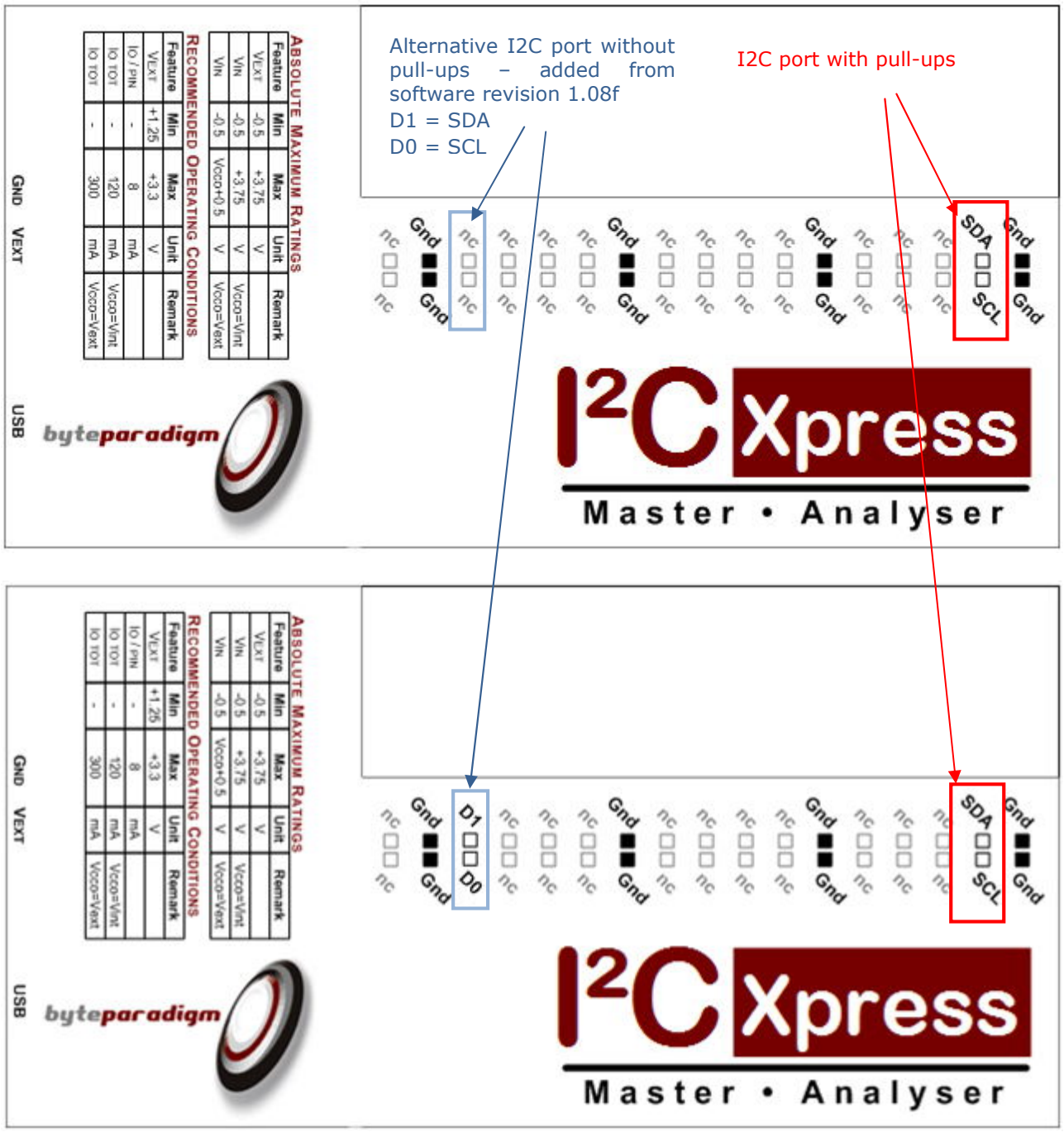
The **I²C interface** connects the I²C Xpress device to the electronic system under test by means of a set of wires. The standard port is labeled SDA/SCL – this port features pull-ups.

From software version 1.08f, an alternative I²C port is available. It is labeled "D1/D0" on devices delivered after 1.08f release (Feb. 2010). On older devices, D1/D0 are labeled "nc" – and located next to the left hand ground pins of the connector (see pictures below). D1 is used for SDA and D0 is used for SCL.

Figure 7: System connector pin groups allocation

The pin mapping slightly differs if you use device hardware revision 02 or 03:

Figure 8: System connector pin groups allocation for HW revision 02 or 03



Besides these 2 groups, the other pins are voltage and GND pins and cannot be used for functional signalling (refer to section 3.3).

Table 1 : I²C Xpress pins

Pin name	Direction	Description / Options
V_{EXT}	-	External power supply pins – refer to section 3.3
Gnd	-	Ground pins
I²C Xpress used in master and slave modes		
SDA	INOUT	I²C data line with pull-up
SCL	INOUT	I²C clock line with pull-up
D1	INOUT	Alternative I²C data line (SDA) without pull-up
D0	INOUT	Alternative I²C clock line (SCL) without pull-up
SDA / SCL pull-up value	-	2.2 kΩ for device hardware revision 01 4.7 kΩ for device hardware revisions 02 or 03

4.1.2 I²C interface clock

I²C Xpress always uses the SCL I/O line to generate and receive the I²C port clock.

Additionally, when used as an **analyzer**, I²C Xpress oversamples SDA and SCL signals with an internal clock.

The I²C Xpress device clock frequency is defined through the host software. Table 2 summarises the available frequency ranges, and how to set them.

Table 2: System interface clocks frequency ranges

Clock	Frequency range	Description / Options
Internal sampling clock	763 Hz to 50 MHz	The I²C Xpress device contains a clock divider unit, programmable with a 16 bits register. If ClkDiv is the value of this register, the achieved clock frequency is: frefclk / (ClkDiv + 1)
I²C clock (SCL)	800 Hz to 10 MHz	The 8PI control panel software provides specific controls to select predefined I²C speed modes (standard, fast, fast+[2])

4.1.3 I²C interface performance

The maximum clock rate for the system connector signals is 50 MHz. Actual use with the 8PI Control Panel limits operation to 10 Mbps, which is large enough for I²C protocol.

[2] Please contact support@byteparadigm.com for high speed 3.4 Mbps availability and support.

5 DC and Switching Characteristics

5.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Description	Conditions	Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{INT}	-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{EXT}	-0.5	V_{CCO}+0.5	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to V_{INT} or V_{EXT} when, respectively, the internal or external supply source is selected (refer to section 3.3 for more details on the powering scheme).

5.2 Recommended operating conditions

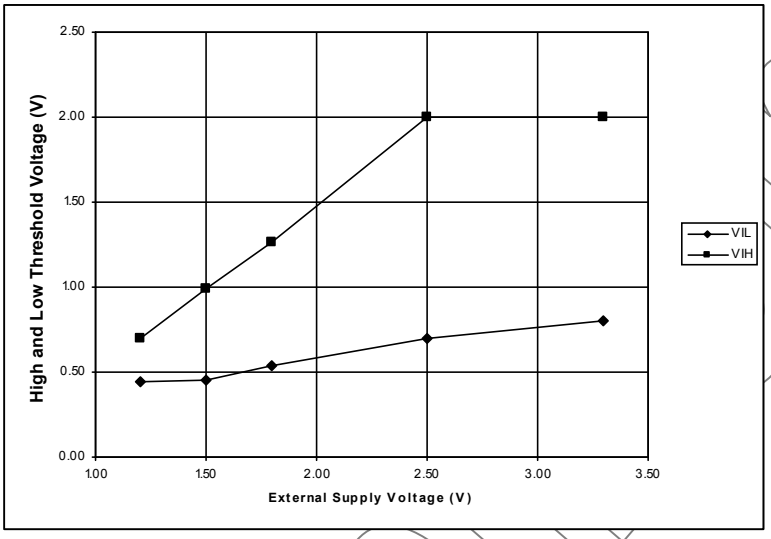
Table 4: Recommended operating conditions

Symbol	Description		Min	Typ	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		+1.8		+3.3	V
I_{CCO}	Quiescent supply current for any user I/O pin.		-		8	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{INT}	-		120	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{EXT}	-		300	mA
T_{OP}	Operating ambient temperature		0		45	°C
V_{IH}[2]	Logic high voltage threshold	V_{CCO}[1] = V_{INT}	2.0		-	V
V_{IL}[2]	Logic low voltage threshold	V_{CCO}[1] = V_{INT}	-		0.8	V
Rpu	Pull-up resistor value on SDA and SCL pins	Hardware revision 01	-	2.2	-	kΩ
Rpu	Pull-up resistor value on SDA and SCL pins	Hardware revision 02 or 03	-	4.7	-	kΩ

Notes:

1. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to VINT or VEXT when, respectively, the internal or external supply source is selected.
2. Refer to Figure 9 for the V_{IH} and V_{IL} threshold voltage when the external supply voltage is selected.

Figure 9: **User I/O input threshold voltage vs external supply voltage**



5.3 System Performance

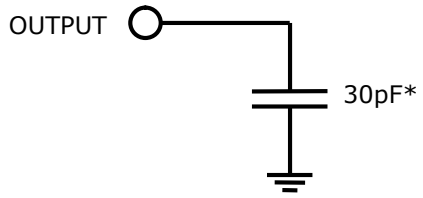
Table 5: **Data throughputs**

Description	Min	Typ.	Max	Unit
USB 2.0 interface total throughput	-	-	480 60	Mbps MByte/s
USB 2.0 interface useful throughput for data	-	-	48	MByte/s
User I/O operating frequency[3]	-	-	50	MHz
I²C interface burst data throughput	-	-	50	Mbit/s

[3] Maximum ratings supported by the device. Actual use does not exceed I²C protocol specification.

5.4 Switching Characteristics

Figure 10: Tests conditions



* The capacitive load includes the measurement probe capacitance

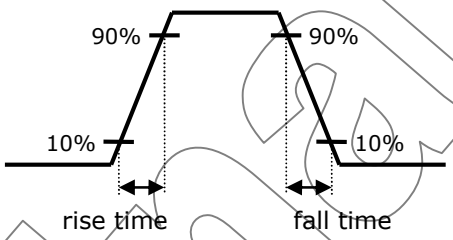


Table 6: Clock frequencies, rise and fall time and skews

Symbol	Description	Min	Typ	Max	Unit
f_{SCL}	I²C clock frequency	763 Hz	-	10 MHz	
T_{SCL}	I²C clock period	100	-	1,250,000	ns
t_{skw} [1]	Skew between SCL and SDA	T_{SCL}/4 - 400	T_{SCL}/4 -50	T_{SCL}/4 +300	ps
t_{lh} [3]	Output pin rise time	-	-	300	ns
t_{hl} [3]	Output pin fall time	-	-	300	ns

Notes:

1. The skew is measured taking SCLK as reference (pin P21 on the user's interface connector). It represents the offset between the reference and all the other data output pins.
2. When SCLK is inverted, the offset with the output data lines is incremented by T/2, with T equal to the output clock period.
3. Rise (10%-90%) and fall (90%-10%) time measured with internal supply voltage selected (+3.3V).

Figure 11: Skew between SCL and the output lines

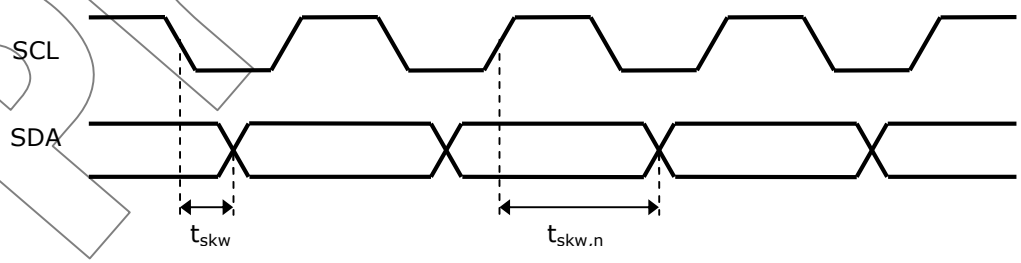


Figure 12: I²C Xpress master switching characteristics

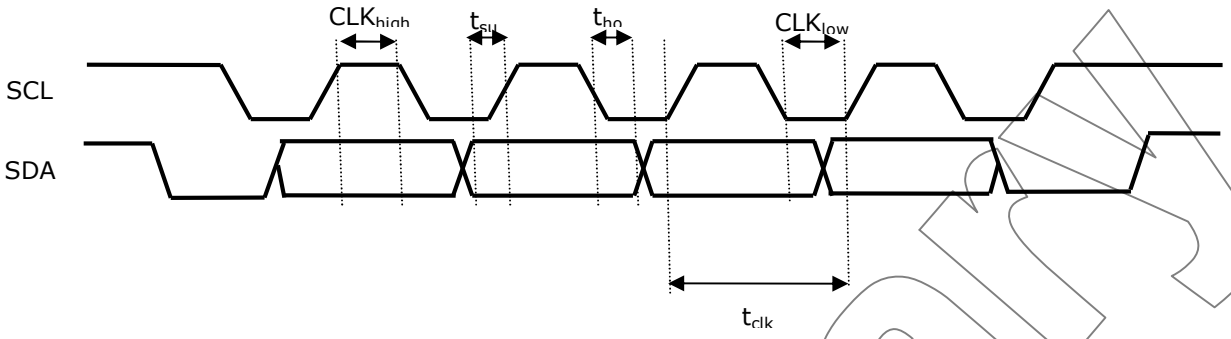


Table 7: I²C Xpress master timing parameters

Symbol	Description	Min	Typ	Max	Unit
CLK_{high}	SCL clock high period				
CLK_{low}	SCL clock low period				
t_{scl}	Clock period	100	-	1,250,000	ns
t_{su}	Data transition to SCL high	5.6	-	-	ns
t_{ho}	SCL low to data transition	0	-	-	ns