



Wave Generator Xpress

Data sheet



Table of Contents

Table of Contents	2
Table of Tables	2
Table of Figures	2
References	4
Revision history	4
1 Features	5
2 Wave Generator Xpress Overview	5
3 Connecting the Wave Generator Xpress	6
3.1 Wave Generator Xpress at a glance	6
3.2 Minimum Host PC requirements	7
3.3 Operating power	7
3.4 USB and system interface connections	8
3.5 Hot plug and play.....	8
4 Wave Generator Xpress functional description.....	9
4.1 Flexible system interface.....	9
4.1.1 Data / Control partition, allocation and configuration.....	9
4.1.2 System interface clocks	10
4.1.3 I ² C bus control dedicated signal lines	11
4.1.4 System interface performance	11
5 DC and Switching Characteristics	12
5.1 Absolute maximum ratings.....	12
5.2 Recommended operating conditions	12
5.3 System Performance	13
5.4 Switching Characteristics	14
5.4.1 Sampling Data Using the Internal Clock.....	15
5.4.2 Sampling Data Using the External Clock	15

Table of Tables

Table 1: Control / Data signals definition	10
Table 2: System interface clocks frequency ranges	11
Table 3: Maximum data depth per run.....	11
Table 4: Absolute maximum ratings	12
Table 5: Recommended operating conditions.....	12
Table 6: Data throughputs	13
Table 7: Clock frequencies, rise and fall time, skews	14
Table 8: Switching characteristics for the internal clock mode	15
Table 9: Switching characteristics for the external clock mode.....	16

Table of Figures

Figure 1: Wave Generator Xpress	5
Figure 2: Wave Generator Xpress overview.....	6
Figure 3: Wave Generator Xpress power source selection	7
Figure 4: System connector external power supply pins	8
Figure 5: USB mini-B to USB type A cable	8
Figure 6: System connector pin groups allocation	9
Figure 7: User I/O input threshold voltage vs external supply voltage	13
Figure 8: Tests conditions.....	14

Wave Generator Xpress

Data sheet

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Figure 9:	Skew between Clk _{OUT} and data output signals, with clock ratio equal to 1	14
Figure 10:	Switching characteristics for the internal clock	15
Figure 11:	Clock path from Clk _{EXT} to Clk _{INT}	16
Figure 12:	Switching characteristics for the external clock mode.....	17

Wave Generator Xpress

Data sheet



References

- [1] 8PI Control Panel User's Guide (ug_8PIControlPanel.doc)
- [2] TCL scripting for ADWG application (ug_ADWGTclLib.pdf)
This document explain how to use the ADWG mode of operation using the Tcl scripting interface. It also contains a complete list of all available procedures to operate in ADWG mode.
- [3] C/C++ library for ADWG application (ug_ADWGCLib.pdf)
This document describes how to use the C/C++ library provided with the ADWG application.

Revision history

Version	Date	Description
1.00	March 2008	First release

1 Features

- ▶ High-speed USB 2.0 host interface (full-speed 12 Mbps and high-speed 480 Mbps)
- ▶ 16 output data lines for data streaming from the PC
- ▶ 6 control lines for in/out clocking, triggering and repetitive sequence generation
- ▶ 50 MHz maximum frequency on all signals
- ▶ Maximum burst throughput: 100 MByte/s
- ▶ Maximum continuous throughput: 48 MByte/s¹
- ▶ Indicative actual sustainable continuous throughput: 11 MByte/s²
- ▶ 16 kB internal memory buffer
- ▶ 'On-the-fly operation' – limited to 100 MByte and 100 MSample total data depth per run
- ▶ Selectable internal (USB bus) or external power supply for I/Os voltages
- ▶ I/O voltage from 1.2V to 3.3V (extensible with plug-in hardware modules)
- ▶ Delivered with the 8PI Control Panel software suite, ADWG mode of operation license included
- ▶ Applications:
 - ASIC, FPGA, DAC and digital board verification / characterisation;
 - Automated stimulus generation;
 - Data source emulation
 - Bus master emulation;
 - System debug and system prototype access;
 - IP evaluation;

2 Wave Generator Xpress Overview

Byte Paradigm **Wave Generator Xpress** (**Error! Reference source not found.**) is a USB 2.0 high speed digital pattern generator or arbitrary digital waveform generator. It generates arbitrary digital stimuli on up to 16 bits, 100 MByte and 100 MSample data depth per run, at up to 50 MSample/s.

It is typically used to send arbitrary stimuli to your board or chip prototype, exercise custom digital interfaces and produce arbitrary digital sample streams to your system under test. Wave Generator Xpress is a convenient, robust and compact personal pattern generator for a wide variety of test and debug tasks on electronic systems.

Wave Generator Xpress is controlled with the **8PI Control Panel Software** freely licensed with the **ADWG** (Arbitrary Digital Waveform Generator) mode of operation. With its multiple graphical and programming (TCL/tk and C/C++) interfaces, you have many flexible options to generate stimuli, from binary or text file to whole algorithms programmed in Tcl/tk, C/C++, Visual Basic and many others.

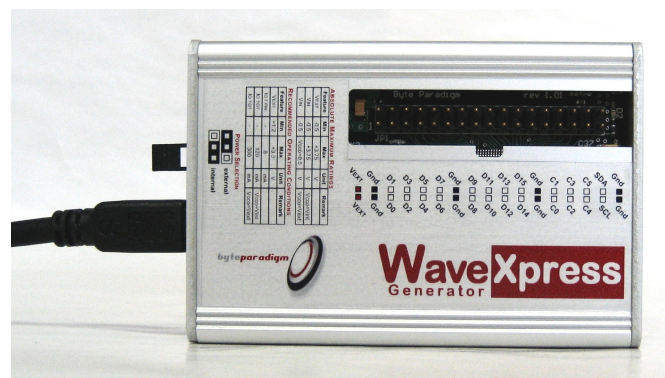


Figure 1: Wave Generator Xpress

¹ The limiting factor is the host computer controlling the Wave Generator Xpress. 48 MByte/s is the maximum throughput achievable by the USB 2.0 connection hardware implementation.

² Informative only – depends on the host PC. Result of a test with the ADWG application with a Pentium 4 3 GHz host computer.



3.2 Minimum Host PC requirements

Wave Generator Xpress connects to any PC using Microsoft Windows XP or Windows Vista operating systems through a USB 1.x or USB 2.0 port connector. For best performance, it is however recommended to use a USB 2.0 port, high-speed mode (480 Mbps).

3.3 Operating power

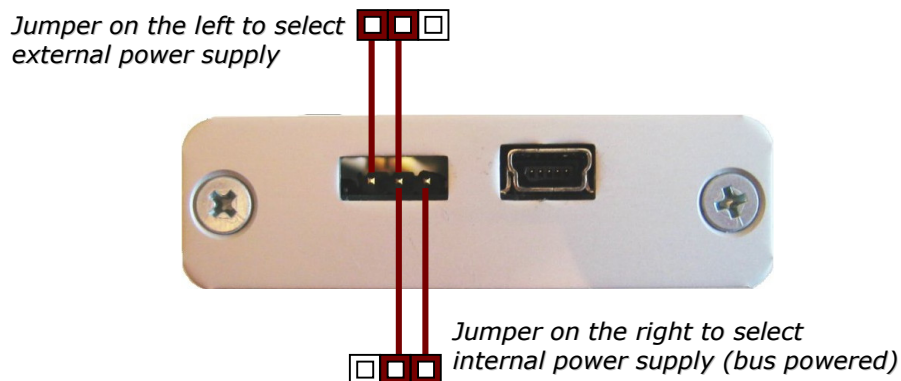
The main power supply of the Wave Generator Xpress is taken from the USB bus to provide the necessary voltage to the device core. The system interface can be powered either from the USB bus (internal power supply mode) or from an external power supply.

When the internal power supply mode is selected, the Wave Generator Xpress is then fully bus powered and operates without any external power supply. In this mode, the voltage level of the system interface is fixed to +3.3V (Refer to section "5 DC and Switching Characteristics" for more details on the compatible I/O voltage levels for the system connector).

The system connector can however operate at different voltage level between +1.2V and +3.3V. To enable this mode, an external power supply must be applied to the system connector V_{EXT} pins and the external supply mode must be selected.

A **power supply source selection jumper** is located at the side of the Wave Generator Xpress, on the left of the Mini-B USB connector. When the two left pins of the connector are shorted, the external mode is selected and an external power supply has to be provided by the user (Refer to Figure 3). When the two right pins are shorted, the internal mode is selected.

Figure 3: Wave Generator Xpress power source selection



To switch the power supply mode the following sequences must be respected.

Enabling the external power mode:

1. Disconnect the device from the USB bus
2. Change the jumper position to select the external mode
3. Connect the system interface GND pins of the system interface to the reference of the external power supply.
4. Connect and apply the external power supply to the V_{EXT} pins of the system connector.
5. Connect the device to the USB bus.

Enabling the internal power mode (bus powered):

1. Disconnect the device from the USB bus

Wave Generator Xpress

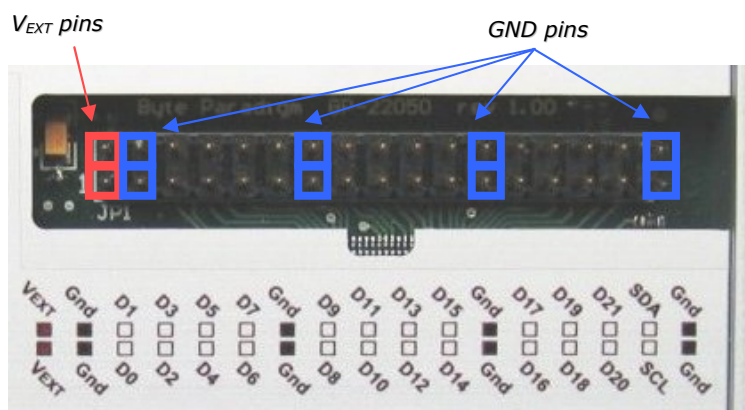
Data sheet



2. Shut down and disconnect the external power supply.
3. Change the jumper position to select the internal mode
4. Connect the device to the USB bus.

i To improve signal integrity it is recommended to connect as many GND pins as possible to the reference ground of the system under test.

Figure 4: System connector external power supply pins



3.4 USB and system interface connections

A 2 meters USB mini-B to USB type A is provided with all Wave Generator Xpress packages (Figure 5).

Figure 5: USB mini-B to USB type A cable



A set of 34 flying lead wires connect the Wave Generator Xpress to the board under test. A standard pin header with 2.54 mm (0.1 inch) pitch must be foreseen on the target board where access is desired (Figure 4). A standard 34 way F-F flat cable (delivered as option) can also be used but offers less flexibility for pin mapping and for the connection of multiple board access points.

3.5 Hot plug and play

The Wave Generator Xpress USB device can be attached and removed from the host computer without having to power-down or reboot. There is a delay after connecting the device to the host system before it is actually functional and reported as one of the Windows devices; during this time, the host software detects the Wave Generator Xpress and programs its hardware settings.



4 Wave Generator Xpress functional description

4.1 Flexible system interface

Features:

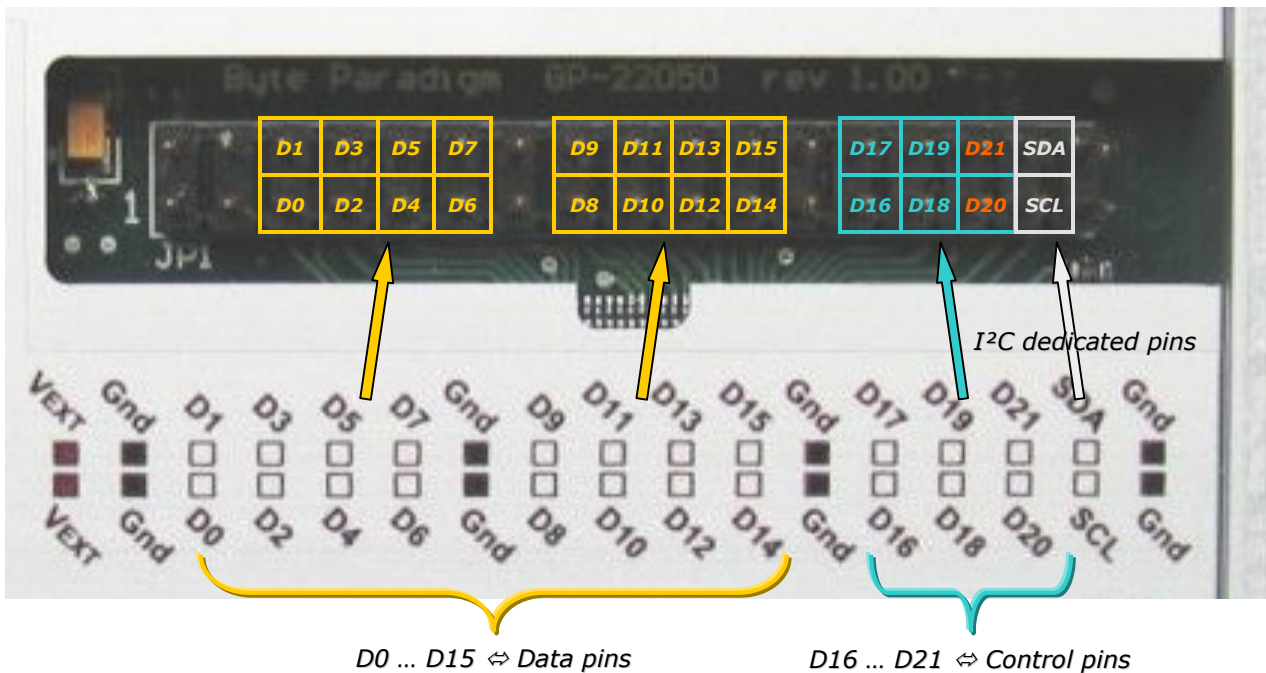
- ▶ Up to **16 data lines** and **6 control lines**;
- ▶ **Individual functional signal allocation** onto the system connector;
- ▶ **Internal or external clocking reference** - 1 specific control input for external clocking;

4.1.1 Data / Control partition, allocation and configuration

The **system interface** connects the Wave Generator Xpress Accelerator to the electronic system under test. For that purpose, a set of flying leads wires ensure the link between the system under test and the Wave Generator Xpress **system connector**. Using flying leads wires offer a 'physical flexibility' for Wave Generator Xpress / system signal mapping.

As depicted on Figure 6, the system connector pins are grouped as **data pins** and **control pins**. The SDA and SCL pins are special control pins used for I²C bus control.

Figure 6: System connector pin groups allocation



Besides these 2 groups, the other pins are voltage and GND pins and cannot be used for functional signalling (refer to section 3.3).

- ▶ **Data pins:** system connector pins labelled from **D0 to D15**.
- ▶ **Control pins:** system connector pins labelled from D16 to D21. Moreover, some control pins have a dedicated use for input and output clock signals, when used:
 - **output clock signal** is mapped onto the **D21** control pin.



- **input reference clock signal** must be mapped onto the **D20** control pin.
- ▶ **I²C pins:** SDA and SCL are specific control pins for I²C bus interfacing.

During Wave Generator Xpress operation, a set of functional signals are defined to access the system under test, according to the chosen application. These signals must be considered either as data signals or as control signals. **Within each group** (data or controls), the connector pins can be reserved for any functional signal defined to access the system under test. Control and data signals are defined according to their purpose within a given access protocol and the possibility to update/visualise them through the host software; their respective characteristics are summarised in Table 1.

Table 1: Control / Data signals definition

Signal type	Direction	Description / Usage
Control	Output	The user can define one or several repetitive output control sequences managed autonomously by the Wave Generator Xpress Accelerator. For example, output control sequences are used for repetitive signal sequences for which timing is critical.
Control	Input	The user can define one or several input control sequences used as event to trigger an autonomous response from the Wave Generator Xpress. The history of the inputs on the control lines cannot be collected by the host computer through the USB 2.0 connection. For example, input control sequences are used as start trigger to collect data (on the data pins) and send them to the host computer.
Data	Output	The data sent to the Wave Generator Xpress system connector are defined and updated by the user through the host software. Repetitive sets of data can be defined as well and memorised in the Wave Generator Xpress Accelerator embedded memory.

4.1.2 System interface clocks

Two optional clock signals can be mapped onto the system connector:

- ▶ An **input clock signal**: this clock signal comes from the system under test and is used as the reference clock signal to generate and sample data and controls onto the system connector. If this clock signal is used, it must be mapped onto the system connector **D20** control pin. Alternatively, if no external reference clock signal is provided, the Wave Generator Xpress internal clock signal is used.
- ▶ An **output clock signal**: when a clock reference has to be provided to the system under test by the Wave Generator Xpress, this signal is conventionally mapped onto the system connector **D21** pin.

The Wave Generator Xpress Accelerator clock frequencies are defined through the host software. Table 2 summarises the available frequency ranges, and how to set them.



Table 2: System interface clocks frequency ranges

Clock	Frequency range	Description / Options
External reference clock	$F_{EXT} / 2^{16}$ to F_{EXT} ; $F_{EXT} \text{ max} = 50 \text{ MHz}$	
Internal reference clock	763 Hz to 50 MHz	The Wave Generator Xpress Accelerator contains a clock divider unit, programmable with a 16 bits register. If ClkDiv is the value of this register, the achieved clock frequency is: $f_{refclk} / (\text{ClkDiv} + 1)$
Output clock (D21)	- to 50 MHz	

4.1.3 I²C bus control dedicated signal lines

The SDA and SCL pins are pulled-up with a resistor of 2.2k Ω , for I²C protocol interfacing. Please contact support@byteparadigm.com for more information about this feature.

4.1.4 System interface performance

The maximum clock rate for the system connector signals is 50 MHz. When all the system interface signals are used, the maximum achievable throughput is: 16 bits x 50 MHz = 800 Mbps, that is to say **100 MByte/s**.

It is important to note that this throughput can be sustained as long as sufficient data are available. This mainly depends on the local buffering memory available for the data transfer. Up to 16 kB memory can be allocated. However, because the Wave Generator Xpress performs 'on-the-fly' data transfer from the host PC, the total data depth available is in reality limited to 100 MByte and 100 MSample, if the data transfer rate is held below a PC-dependant level. The 'sustainable continuous throughput' is an indicative figure mentioned with the Wave Generator Xpress performance figures. It is the maximum sustainable throughput for 'infinite' data transmission to and from the host PC. Tests conducted on a Pentium 4, 3GHz PC show sustainable throughput up to 11 MByte/s.

Table 3: Maximum data depth per run

Number of pins used on the connector	Maximum data depth per run (Samples)	Maximum data depth per run (Byte)
1 to 8	100 MSample	100 MByte
9 to 16	50 MSample	100 MByte



5 DC and Switching Characteristics

5.1 Absolute maximum ratings

Table 4: Absolute maximum ratings

Symbol	Description	Conditions	Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	$V_{CCO}^2 = V_{INT}$	-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	$V_{CCO}^2 = V_{EXT}$	-0.5	$V_{CCO}+0.5$	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. V_{CCO} is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to V_{INT} or V_{EXT} when, respectively, the internal or external supply source is selected (refer to section 3.3 for more details on the powering scheme).

5.2 Recommended operating conditions

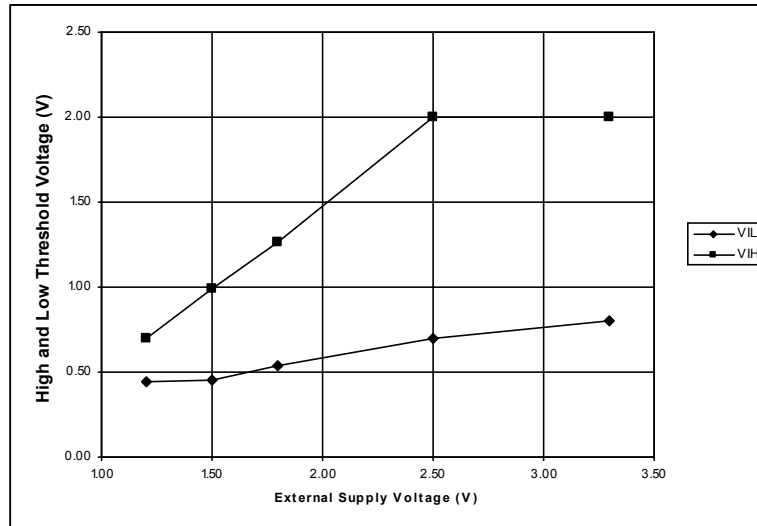
Table 5: Recommended operating conditions

Symbol	Description		Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		+1.2	+3.3	V
I_{CCO}	Quiescent supply current for any user I/O pin.		-	8	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	$V_{CCO}^1 = V_{INT}$	-	120	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	$V_{CCO}^1 = V_{EXT}$	-	300	mA
T_{OP}	Operating ambient temperature		0	45	°C
V_{IH}^2	Logic high voltage threshold	$V_{CCO}^1 = V_{INT}$	2.0	-	V
V_{IL}^2	Logic low voltage threshold	$V_{CCO}^1 = V_{INT}$	-	0.8	V

Notes:

1. V_{CCO} is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to V_{INT} or V_{EXT} when, respectively, the internal or external supply source is selected.
2. Refer to Figure 7 for the V_{IH} and V_{IL} threshold voltage when the external supply voltage is selected.

Figure 7: User I/O input threshold voltage vs external supply voltage



5.3 System Performance

Table 6: Data throughputs

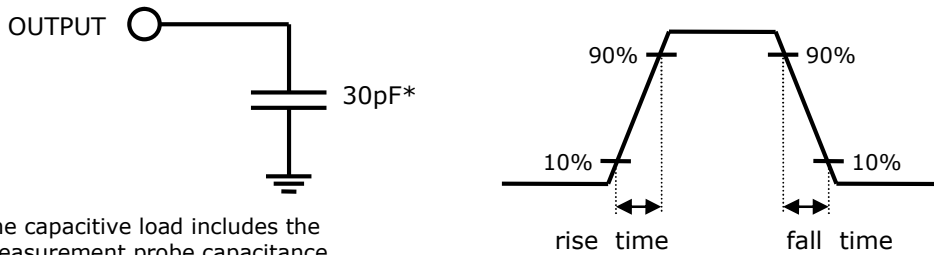
Description	Min	Typ.	Max	Unit
USB 2.0 interface total throughput	-	-	480 60	Mbps MByte/s
USB 2.0 interface throughput within Wave Generator Xpress	-	-	48	MByte/s
User I/O operating frequency	-	-	50	MHz
System interface burst throughput ¹	-	-	100	MByte/s
System interface continuous throughput ^{2,3}	-	11	-	MByte/s

Notes:

1. The burst throughput is the performance achievable when performing transfers of 16 Kbytes or less.
2. The continuous throughput is the performance achievable when performing transfers of more than 16Kbytes. The throughput is dependent of the host computer performances. The provided values are given as indicative reachable performance only.
3. There is no limit in the maximum amount of data that can be transferred using the Wave Generator Xpress. Continuous mode is then used to describe transfers larger than the internal device memory. The 8PI Control Panel software delivered with the Wave Generator Xpress limits a single data run to 100 MByte.

5.4 Switching Characteristics

Figure 8: Tests conditions



* The capacitive load includes the measurement probe capacitance

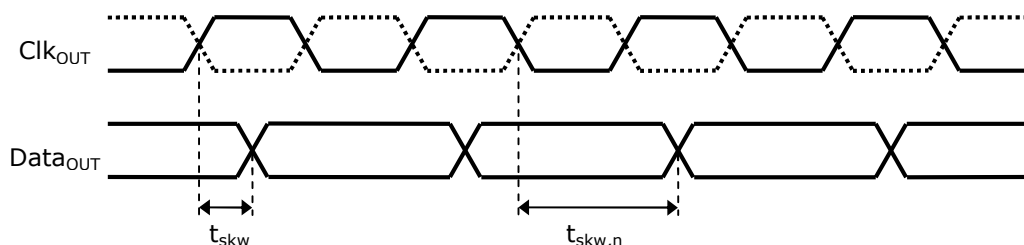
Table 7: Clock frequencies, rise and fall time, skews

Symbol	Description	Min	Typ	Max	Unit
F_{CLKI}	Internal clock frequency	763 Hz	-	50 MHz	
F_{CLKE}	External clock frequency	-	-	50	MHz
F_{CLKO}	Output clock frequency	-	-	50	MHz
t_{skw}^1	Skew between clock out and the output lines when Clk_{OUT} is not inverted	-400	-50	300	ps
$t_{skw,n}^{1,2}$	Skew between clock out and the output lines when Clk_{OUT} is inverted	$T/2-400$	$T/2-50$	$T/2+300$	ps
t_{in}^3	Output pin rise time	2.2	2.7	3.3	ns
t_{hl}^3	Output pin fall time	4.4	5.4	6.6	ns

Notes:

1. The skew is measured taking Clk_{OUT} as reference (pin P21 on the user's interface connector). It represents the offset between the reference and all the other data output pins.
2. When Clk_{OUT} is inverted, the offset with the output data lines is incremented by $T/2$, with T equal to the output clock period.
3. Rise (10%-90%) and fall (90%-10%) time measured with internal supply voltage selected (+3.3V).

Figure 9: Skew between Clk_{OUT} and data output signals, with clock ratio equal to 1





5.4.1 Sampling Data Using the Internal Clock

The Wave Generator Xpress device can operate with an external reference clock signal provided by the user (applied on pin P20 of the system connector) or with the internally generated clock. Clk_{OUT} is the image of the internal clock. Clk_{INT} is the reference clock. All timing values in this section are measured from Clk_{INT} rising edge.

When the device is used in analyser mode, data can be sampled on Clk_{INT} rising or falling edge. The setup and hold time are measured relatively to the edge used to sample the data (refer to Figure 10).

i Refer to [1] for more information on how to change the sampling edge and clock polarity.

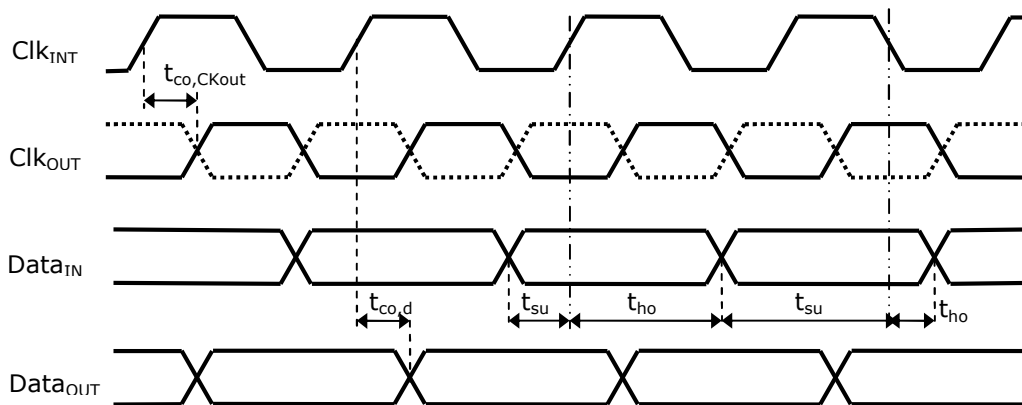
Table 8: Switching characteristics for the internal clock mode

Symbol	Description	Min	Max	Unit
$t_{co,CKout}^1$	Clock to output delay for signal Clk_{OUT}	2.0	6.0	ns
$t_{co,d}^1$	Clock to output delay for signal Clk_{OUT}	2.0	6.0	ns
t_{su}^2	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho}^2	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

Notes:

1. Values computed from used components manufacturer datasheet.
2. Setup and hold values are independent of the Clk_{INT} edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.

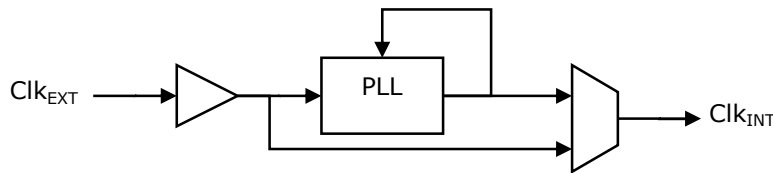
Figure 10: Switching characteristics for the internal clock



5.4.2 Sampling Data Using the External Clock

When the Wave Generator Xpress device operates in the external clock mode, the user supplied clock signal can follow two different clock paths to become the internal reference clock. One of the two paths includes a PLL to shorten the propagation delay. The internal clock is used as reference. All setup and hold values in this section are measured from the rising edge of to this clock Clk_{INT} .

Figure 11: Clock path from Clk_{EXT} to Clk_{INT}



When the device is used in analyser mode, data can be sampled on Clk_{INT} rising or falling edge. The setup and hold time are measured relatively to the edge used to sample the data (refer to Figure 12). When operating in arbitrary generator mode, all the outputs are generated on Clk_{INT} rising edge. Inverting the polarity of Clk_{OUT} does not change the edge used to send data out of the device.

Table 9: Switching characteristics for the external clock mode

Symbol	Description	Min	Max	Unit
$t_{co,CKout}^3$	Clock to output delay for signal Clk _{OUT} from reference clock Clk _{INT} .	2.0	6.0	ns
$t_{co,d}^3$	Clock to output delay for output data lines from reference clock Clk _{INT}	2.0	6.0	ns
t_{pce}^3	Delay from Clk _{EXT} input pin to the internal reference clock Clk _{INT} when no PLL is inserted in the clock path.	2.7	8.4	ns
$t_{pcep}^{1,3}$	Delay from Clk _{EXT} input pin to the internal reference clock Clk _{INT} when the PLL is inserted in the clock path.	1.8	4.5	ns
t_{su}^2	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho}^2	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

Notes:

1. The PLL can only be used for clock frequencies greater than or equal to 20MHz (refer to [1] for more details).
2. Setup and hold values are independent of the Clk_{INT} edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.
3. Values computed from used components manufacturer datasheet.



Figure 12: Switching characteristics for the external clock mode

