GP-241xx

Data sheet

Revision 1.03 - December 2011

Table of Contents

Table of Tables

Table of Figures

References

[1]

Revision history

Version	Date	Description
1.00	November 2009	First release
1.01	February 2010	Updated I2C port description
1.02	November 2010	1.02 version covers all GP-241xx devices. This is an update of the 1.01 version of the GP-24100 data sheet extended for GP-24116 and GP-24132 devices.
1.03	December 2011	Added dimensions of device

1 Features

- High-speed USB 2.0 host interface (full-speed 12 Mbps and high-speed 480 Mbps)
- Configurable system interface: up to 16 bidirectional data and 8 control signals[1]
- System interface frequency up to 100 MHz
- Maximum burst throughput: 200 MByte/s
- Maximum continuous throughput: 48 MByte/s[2]
- Indicative actual continuous throughput: 11 MByte/s to 30 MByte/s[3]
- 8 MByte (GP-24100), 16 MByte (GP-24116) or 32 MByte (GP-24132) internal memory buffer
- 'On-the-fly operation' – allowing up to 100 MByte total depth / run
- Selectable internal (USB bus) or external power supply for I/Os voltages
- System interface operating from +1.8V to +3.3V (extensible with plug-in hardware modules).
- Delivered with the 8PI Control Panel software suite, including: documentation, drivers and upgradeable host control software
- Provides multiple and flexible bidirectional access points to a system-on-board under test.
- Applications[4]:
  - ADWG (Arbitrary Digital Waveform Generator) / Digital Pattern Generator;
  - Logic analyser
  - Board access through serial protocols: SPI, I²C, I²S, RS232, …
  - 8 bits/16 bits microcontroller interface;
  - Bus master emulation;
  - SRAM, flash interface;
  - System debug and system prototype access;
  - IP evaluation;
  - Recorder/player tools.
  - JTAG (IEEE 1149.1) access;

2 GP-241xx Overview

Byte Paradigm GP-241xx devices (Figure 1) are set of a high-speed programmable bidirectional interfaces that allows the stimulation and the analysis of digital electronic systems.

Connected to a PC through a USB 2.0 interface and using a fully programmable hardware accelerator, GP-241xx devices enable a flexible and powerful access to electronic system boards and electronic devices under test.

The GP-241xx can be turned into an arbitrary digital pattern generator, logic analyser or serial protocol master / anlyser, that fits in 16

Figure 1: GP-24100

[1] Actual direction setting for each pin depends of the used mode of operation
[2] The limiting factor is the host computer controlling the GP-24100. 48 MByte/s is the maximum throughput achievable by the USB 2.0 connection hardware implementation.
[3] Informative only – depends on the host PC.
[4] Each application requires proper mode of operation. Please contact Byte Paradigm to check about modes of operation roadmap and availability.

address/data lines and 6 control lines, up to 100 MHz (200 MByte/s burst performance).
According to the device model, a total internal memory of 8 MByte, 16 MByte or 32 MByte is available.

Device	***Data/Pattern width***	***Max. frequency***	***Emb. Memory***
GP-24100	16 bits	100 MHz	8 MByte
GP-24116	16 bits	100 MHz	16 MByte
GP-24132	16 bits	100 MHz	32 MByte

GP-241xx devices are able to sustain a theorical continuous throughput of 48 MByte/s[5]. The actual throughput for continuous transfer depends on the host PC performances and can be expected between 11 MByte/s and 30 MByte/s[6]. For most usages – and only for 3.3V I/O standards –GP-241xx device is powered directly through the host PC USB connection, enabling a very quick device setup. Additionally, an external power supply can be connected to the GP-241xx devices when higher current must be sinked through the system or when another I/O voltage is required.

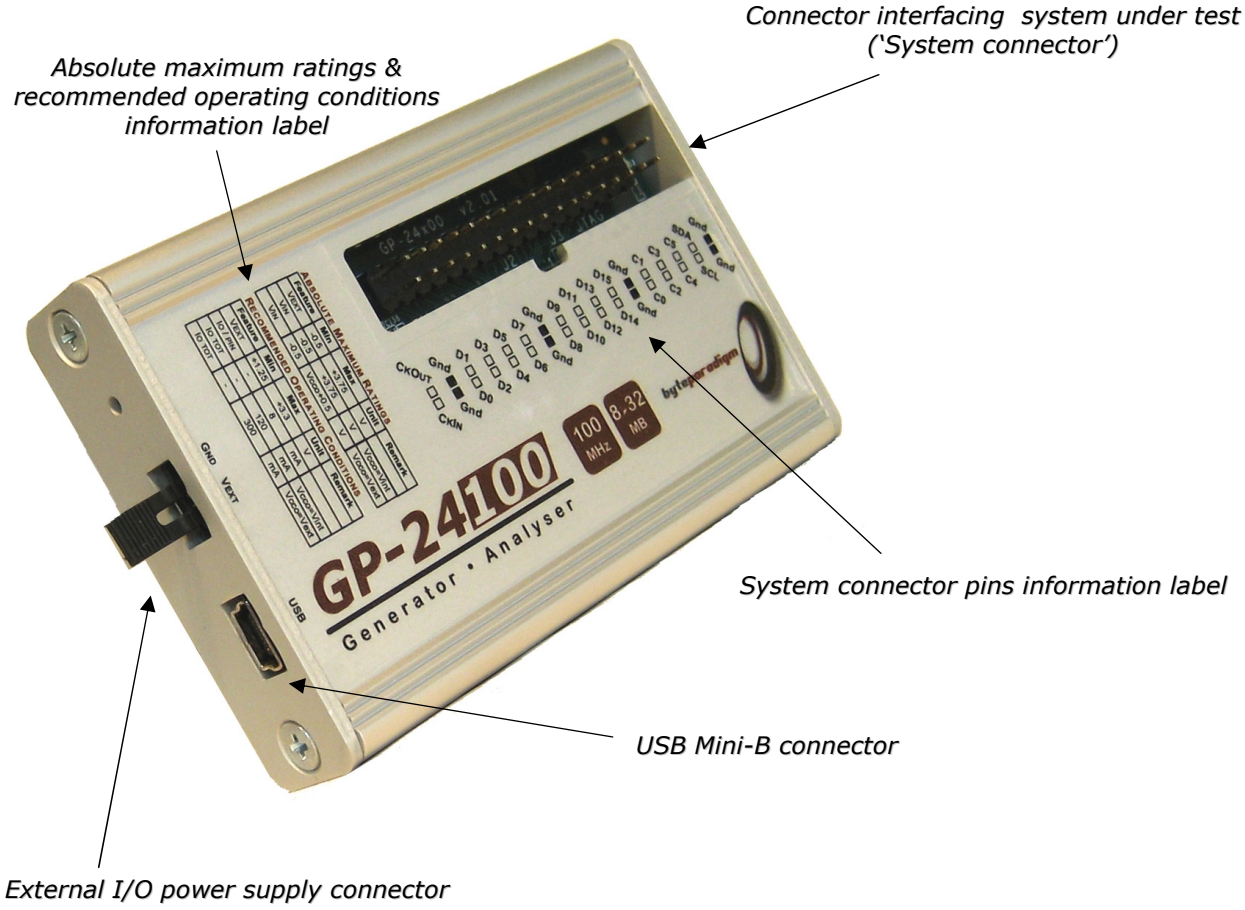
Figure 2 : GP Series - GP-22050 and GP-241xx family

[5] Actually, the USB 2.0 high speed connection throughput is 60 MB/s (480 Mb/s); this bandwidth must be shared between the data and the USB protocol controls.
[6] Result of a performance test with a Pentium 4 3GHz PC, GP-24100 configured as a pattern generator.

3 Connecting the GP-241xx

3.1 GP-241xx at a glance

Figure 3: GP-241xx overview – GP-24100 taken as example



3.2 Case & dimensions

Anodised aluminium case (WxLxH): **55x80x16 mm**

3.3 Minimum Host PC requirements

GP-241xx connects to any PC using Microsoft Windows XP / Windows Vista / Windows 7 operating systems through a USB 2.0 port connector.

3.4 Operating power

The main power supply of the GP-241xx is taken from the USB bus to provide the necessary voltage to the device core. The system interface can be powered either from the USB bus (internal power supply mode), either from an external power supply, to control the voltage level used by the device I/Os connected to a system under test.

When the internal power supply mode is selected, the GP-241xx is fully bus-powered and operates without any external power supply. In this mode, the voltage level of the system interface is fixed to +3.3V (Refer to section "5 DC and Switching Characteristics" for more details on the compatible I/O voltage levels for the system connector).

The system connector can however operate at different voltage level between +1.8V and +3.3V.

An external power supply connector is located at the side of the device. It is protected with a jumper. This power connector is labelled "GND VEXT". **! Respect the connector polarity when using !**

An internal automatic switching mechanism holds the I/O voltage between 1.2V and 3.3V: when the supplied external I/O voltage drops below 1.2V or rises over 3.3V, the I/O voltage is automatically switched to the internal 3.3V voltage. This mechanism is not a full voltage protection: the user MUST respect the absolute maximum ratings, as specified at section 5.1.

Enabling the external power mode:

1. Disconnect the device from the USB bus
2. Remove the jumper from the VEXT connector
3. Connect and apply the external power supply to the V_{EXT} pins of the system connector **(! respect the polarity, as shown on the label near the connector !)**
4. Connect the device to the USB bus.

Enabling the internal power mode (bus powered):

1. Disconnect the device from the USB bus
2. Shut down and disconnect the external power supply.
3. Connect the device to the USB bus.

Figure 4: GP-241xx external power connector

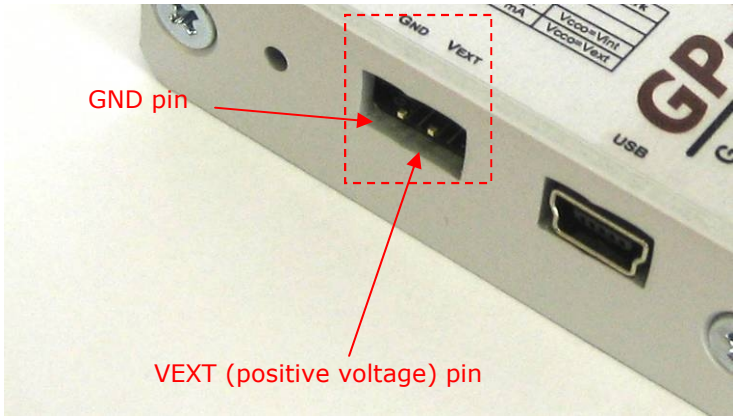
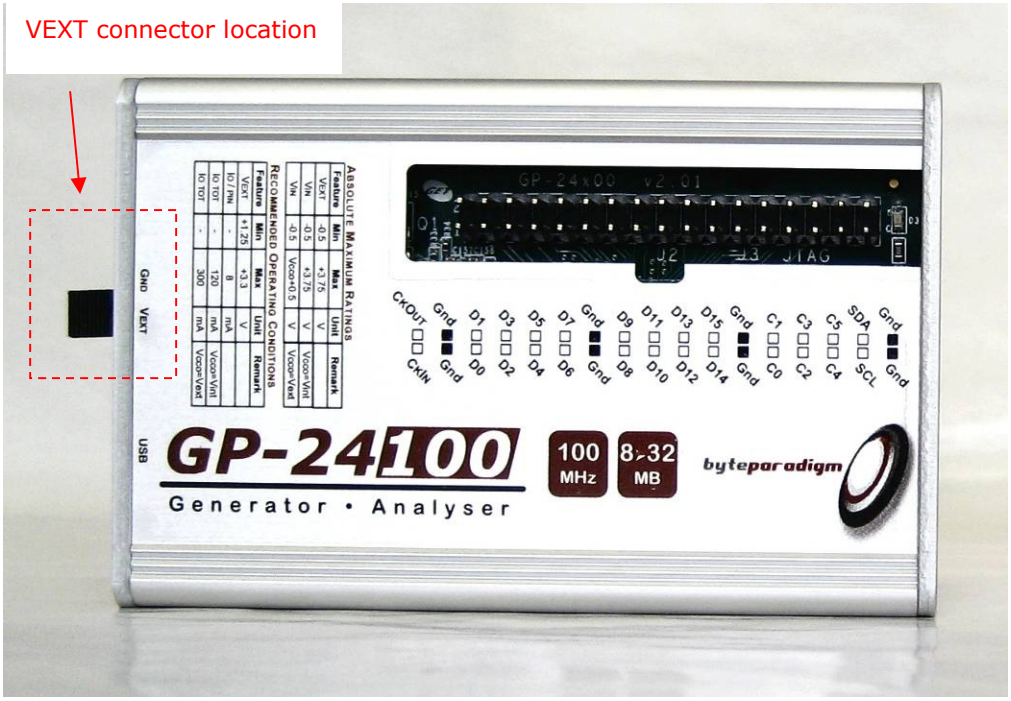


Figure 5: GP-241xx VExt connector location



3.5 USB and system interface connections

A 1.5 or 2 meters USB mini-B to USB type A is provided with all GP-241xx packages (Figure 6).

A set of 34 flying lead wires connect the GP-241xx device to the board under test. A standard pin header with 2.54 mm (0.1 inch) pitch must be foreseen on the target board where access is desired.

Figure 6: USB mini-B to USB type A cable

3.6 Hardware accelerator configuration

As multi-mode / multi-function device, GP-241xx is mode of operation-oriented.
The modes of operation currently available[7] are:

- ADWG : digital pattern generator;
- Analyser : logic analyser;
- SPI : SPI (serial peripheral interface) master and analyser;
- I2C : I²C protocol master and analyser

When used with the 8PI Control Panel software suite, each mode of operation defines a set of functionalities and configures the GP-241xx device for proper operation.

Among others, each mode of operation defines:

- the pins used on the system connector and their direction (in, out or bidir)
- the ability to use some control features such as repetitive sequences or triggers
- the limits to some parameters, such as the maximum clock frequency.

Please refer to 8PI Control Panel user's guide for more information about each mode of operation.

3.7 Hot plug and play

The GP-241xx USB device can be attached and removed from the host computer without having to power-down or reboot. There is a delay after connecting the device to the host system before it is actually functional and reported as one of the Windows devices; during this time, the host software detects the GP-241xx and programs its hardware settings.

[7] *JTAG mode of operation is available as a 'legacy mode' only and is not further developed nor updated.*

4 GP-241xx functional description

4.1 Flexible system interface

Features:

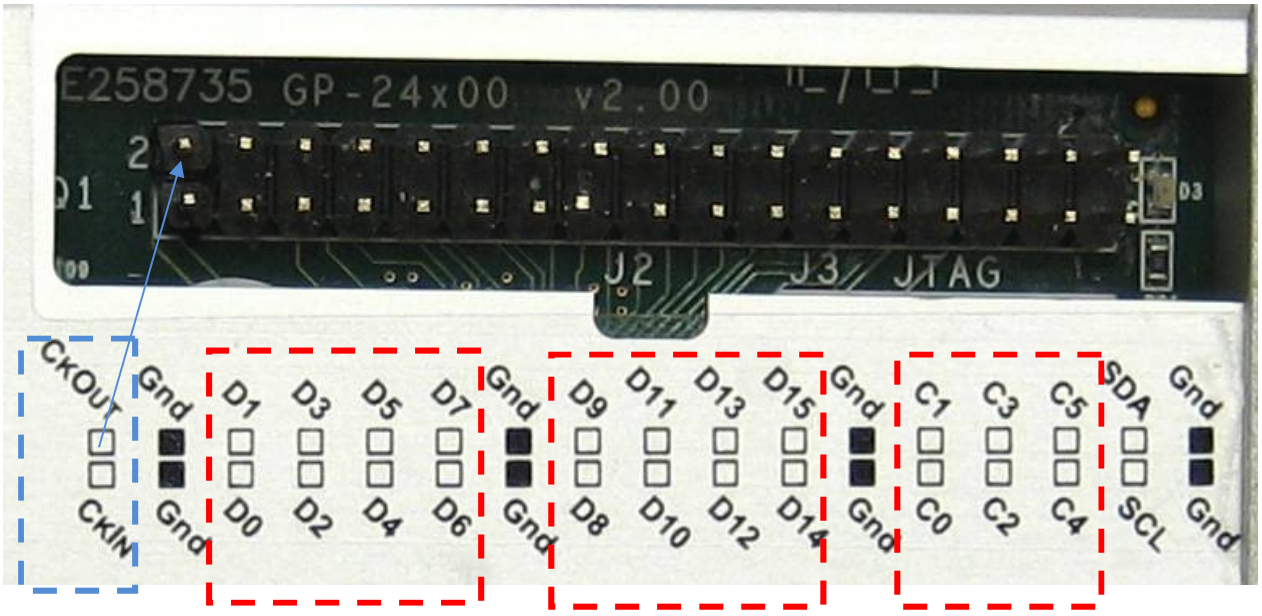
- Up to **16 data lines** and **6 control lines**;
- Mode of operation – oriented : each mode of operation defines specific I/O settings and functionalities.
- Pin direction (in, ouyt, in/out) is configured according to each mode of operation;
- **2 Dedicated external clock I/O (1 in, 1 out)**;
- Dedicated SDA and SCL signals lines with pull-ups for **I²C bus control.**

4.1.1 Data / Control partition, allocation and configuration

The **system interface** connects the GP-241xx to the electronic system under test. A set of flying leads wires is provided for this purpose.

As depicted on Figure 7, the system connector pins are grouped as **data pins** and **control pins.** The SDA and SCL pins are special control pins used for I²C bus control.

Figure 7: System connector pin groups allocation



Dedicated clk in/out pins

Data pins (D0-D15) are used for digital data that transit from / to the host PC through the USB interface.

Control pins (C0 – C5) are used for specific purpose, essentially defined by preloaded settings held in the device hardware. Control pins are used:

- as inputs to define trigger patterns (single- or multiple- bits, level or edge) to (re-)start the device operation;
- as outputs to define a repetitive control sequence or a constant logic level.

The ability to define triggers and/or control sequence onto the control pins depends of the used mode of operation – each mode of operation restricting the set of available functionalities. Please refer to 8PI Control Panel user's guide to find out about each mode of operation functionalities.

4.1.2 System interface clocks

Two optional clock signals can be mapped onto the system connector:

- An **input clock signal**: this clock signal comes from the system under test and is used as the reference clock signal to generate and sample data and controls onto the system connector. If this clock signal is used, it must be mapped onto the system connector **CKIN** dedicated pin. Alternatively, if no external reference clock signal is provided, the GP-241xx internal clock signal is used and the CKIN input pin is left unconnected.
- An **output clock signal**: when a clock reference has to be provided to the system under test by the GP-241xx, this signal is mapped onto the system connector **CKOUT** output pin.

The GP-241xx clock frequencies are defined through the host software. Table 1 summarises the available frequency ranges, and how to set them.

Table 1: System interface clocks frequency ranges

Clock	Frequency range	Description / Options
External reference clock	$F_{EXT} / 2^{16}$ to F_{EXT} ; F_{EXT} max = 100 MHz	
Internal reference clock	763 Hz to 100 MHz	The GP-241xx contains a clock divider unit, programmable with a 16 bits register. If ClkDiv is the value of this register, the achieved clock frequency is: frefclk / (ClkDiv + 1)
Output clock (CKOut)	- to 100 MHz	

4.1.3 I²C bus control dedicated signal lines

The SDA and SCL pins are pulled-up with a resistor of **2.2kΩ**, for I²C protocol interfacing on hardware revision 01.

On hardware revisions 02 or 03, the pull-up resistors value is **4.7 kΩ**.

Alternatively, the D1 (for SDA) and D0 (for SCL) can be used for I2C master / analyzer. These pins do not feature any pull-up resistor. Please refer to the 8PI Control Panel user's guide for more information on how to activate this alternative port (this feature is available from 8PI Control Panel version 1.08f).

4.1.4 System interface performance

The maximum clock rate for the system connector signals is 100 MHz. When all the system interface signals are configured with the same I/O direction, the maximum achievable throughput is: 16 bits x 100 MHz = 1600 Mbps, that is to say **200 MByte/s.**

This throughput can be sustained as long as sufficient data are available. This mainly depends on the local buffering memory available for the data transfer. Up to 32 MB memory can be allocated with GP-24132 device[8]. However, because the GP-241xx performs 'on-the-fly' data transfer to/from the host PC, the total data depth available is in reality limited to 100 MByte, if the data transfer rate is held below a PC-dependant level. The 'continuous throughput' is an indicative figure mentionned with the GP-241xx performance figures. It is the maximum sustainable throughput for 'infinite' data transmission to and from the host PC. Tests conducted on a Dual Core 2 Duo PC show sustainable throughput between 11 MByte/s to 30 MByte/s. This upper limite is in no way guaranteed, as it very much depends on the PC hardware and the applications running on the PC.

[8] This value is 8 MByte for GP-24100 and 16 MByte for GP-24116.

5 DC and Switching Characteristics

5.1 Absolute maximum ratings

Table 2: Absolute maximum ratings

Symbol	Description	Conditions	Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{INT}	-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{EXT}	-0.5	V_{CCO}+0.5	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to V_{INT} or V_{EXT} when, respectively, the internal or external supply source is selected (refer to section 3.4 for more details on the powering scheme).

5.2 Recommended operating conditions

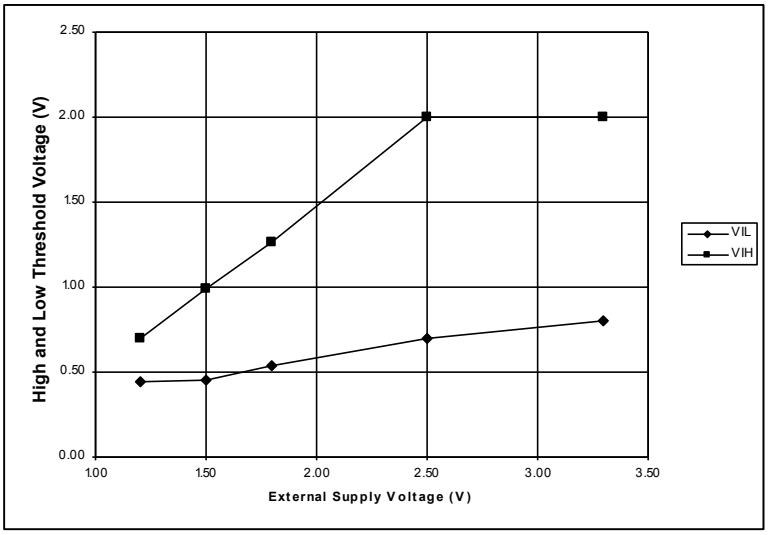
Table 3: Recommended operating conditions

Symbol	Description		Min		Max	Unit
V_{EXT}	External DC supply voltage relative to GND		+1.8	-	+3.3	V
I_{CCO}	Quiescent supply current for any user I/O pin.		-	-	8	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{INT}	-	-	120	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{EXT}	-	-	300	mA
T_{OP}	Operating ambient temperature		0	-	45	°C
V_{IH}[2]	Logic high voltage threshold	V_{CCO}[1] = V_{INT}	2.0	-	-	V
V_{IL}[2]	Logic low voltage threshold	V_{CCO}[1] = V_{INT}	-	-	0.8	V
Rpu	Pull-up resistors on SDA and SCL pins		-	4.7	-	kΩ

Notes:

1. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to VINT or VEXT when, respectively, the internal or external supply source is selected.
2. Refer to Figure 8 for the V_{IH} and V_{IL} threshold voltage when the external supply voltage is selected.

Figure 8: User I/O input threshold voltage vs external supply voltage



5.3 System Performance

Table 4: Data throughputs

Description	Min	Typ.	Max	Unit
USB 2.0 interface total throughput	-	-	480 60	Mbps MByte/s
USB 2.0 interface throughput within GP-241xx	-	-	48	MByte/s
User I/O operating frequency	-	-	100	MHz
System interface burst throughput[1]	-	-	200	MByte/s
System interface continuous throughput[2,3]	-	11	30	MByte/s

Notes:

1. The burst throughput is the performance achievable when performing transfers of max. the total internal memory of the device. This is 8 MByte for GP-24100, 16 MByte for GP-24116 and 32 MByte for GP-24132.
2. The continuous throughput is the performance achievable when performing transfers of more than the total embedded memory of the GP-241xx. The throughput is dependent of the host computer performances. The provided values are given as indicative reachable performance only.
3. Continuous mode is then used to describe transfers larger than the internal device memory. The 8PI Control Panel software delivered with the GP-241xx limits a single data run to 100 MByte.

5.4 Switching Characteristics

Figure 9: Tests conditions[9]

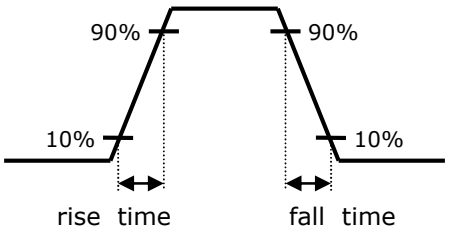


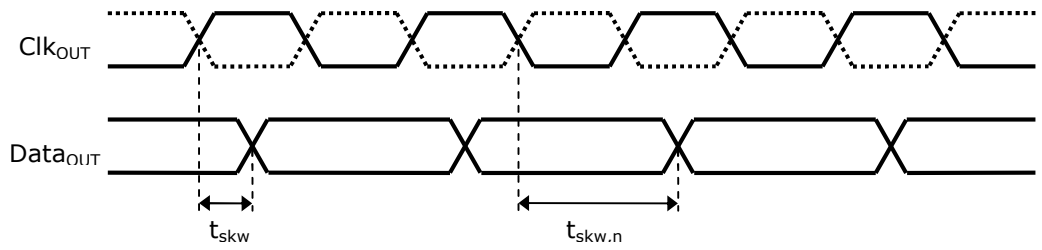
Table 5: Clock frequencies, rise and fall time, skews

Symbol	Description	Min	Typ	Max	Unit
F_{CLKI}	Internal clock frequency	763 Hz	-	100 MHz	
F_{CLKE}	External clock frequency	-	-	100	MHz
F_{CLKO}	Output clock frequency	-	-	100	MHz
t_{skw}[1]	Skew between clock out and the output lines when Clk_{OUT} is not inverted	-400	-50	300	ps
$t_{skw,n}$[1,2]	Skew between clock out and the output lines when Clk_{OUT} is inverted	T/2-400	T/2-50	T/2+300	ps
t_{lh}[3]	Output pin rise time	2.2	2.7	3.3	ns
t_{hl}[3]	Output pin fall time	4.4	5.4	6.6	ns

Notes:

1. The skew is measured taking Clk_{OUT} as reference (pin P21 on the user's interface connector). It represents the offset between the reference and all the other data output pins.
2. When Clk_{OUT} is inverted, the offset with the output data lines is incremented by T/2, with T equal to the output clock period.
3. Rise (10%-90%) and fall (90%-10%) time measured with internal supply voltage selected (+3.3V).

Figure 10: Skew between Clk_{OUT} and data output signals, with clock ratio equal to 1



[9] Measurements done with an output load capacitance of 30 pF including probe capacitance.

5.4.1 Sampling Data Using the Internal Clock

GP-241xx devices can operate with an external reference clock signal provided by the user (applied on pin P20 of the system connector) or with the internally generated clock. Clk_{OUT} is the image of the internal clock. Clk_{INT} is the reference clock. All timing values in this section are measured from Clk_{INT} rising edge.

When the device is used in analyser mode, data can be sampled on Clk_{INT} rising or falling edge. The setup and hold time are measured relatively to the edge used to sample the data (refer to Figure 11).

Refer to [1] for more information on how to change the sampling edge and clock polarity.

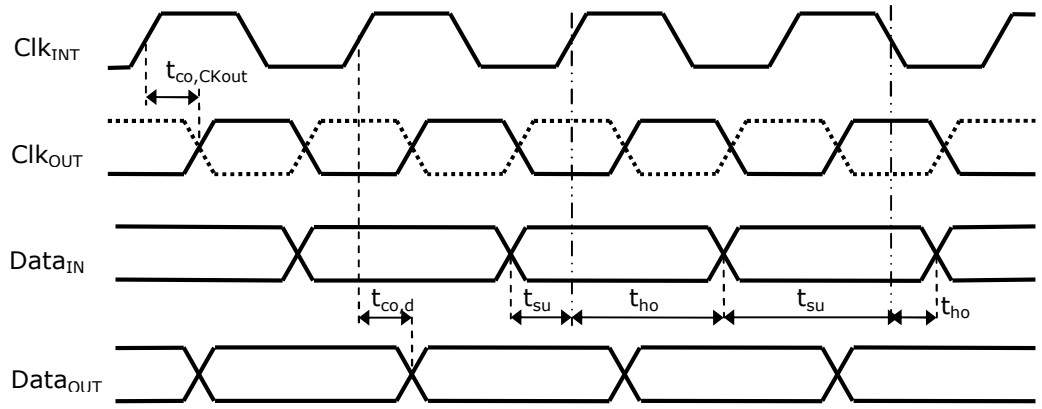
Table 6: Switching characteristics for the internal clock mode

Symbol	Description	Min	Max	Unit
$t_{co,CKout}$ [1]	Clock to output delay for signal Clk_{OUT}	2.0	6.0	ns
$t_{co,d}$ [1]	Clock to output delay for signal Clk_{OUT}	2.0	6.0	ns
t_{su} [2]	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho} [2]	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

Notes:

1. Values computed from used components manufacturer datasheet.
2. Setup and hold values are independent of the Clk_{INT} edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.

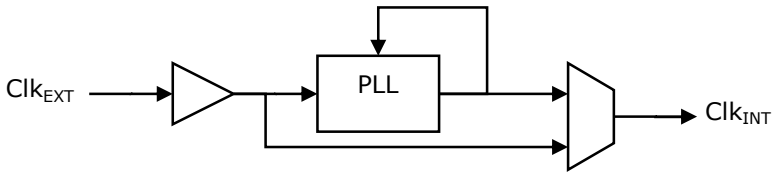
Figure 11: Switching characteristics for the internal clock



5.4.2 Sampling Data Using the External Clock

When the GP-241xx device operates in the external clock mode, the user supplied clock signal can follow two different clock paths to become the internal reference clock. One of the two paths includes a PLL to shorten the propagation delay. The internal clock is used as reference. All setup and hold values in this section are measured from the rising edge of to this clock Clk_{INT}.

Figure 12: Clock path from Clk_{EXT} to Clk_{INT}



When the device is used in analyser mode, data can be sampled on Clk_{INT} rising or falling edge. The setup and hold time are measured relatively to the edge used to sample the data (refer to Figure 13). When operating in arbitrary generator mode, all the outputs are generated on Clk_{INT} rising edge. Inverting the polarity of Clk_{OUT} does not change the edge used to send data out of the device.

Table 7: Switching characteristics for the external clock mode

Symbol	Description	Min	Max	Unit
$t_{co,CKout}$ [3]	Clock to output delay for signal Clk_{OUT} from reference clock $Clk_{INT.}$	2.0	6.0	ns
$t_{co,d}$ [3]	Clock to output delay for output data lines from reference clock Clk_{INT}	2.0	6.0	ns
t_{pce} [3]	Delay from Clk_{EXT} input pin to the internal reference clock Clk_{INT} when no PLL is inserted in the clock path.	2.7	8.4	ns
t_{pcep} [1,3]	Delay from Clk_{EXT} input pin to the internal reference clock Clk_{INT} when the PLL is inserted in the clock path.	1.8	4.5	ns
t_{su} [2]	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho} [2]	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

Notes:

1. The PLL can only be used for clock frequencies greater than or equal to 20MHz (refer to [1] for more details).
2. Setup and hold values are independent of the Clk_{INT} edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.
3. Values computed from used components manufacturer datasheet.

Figure 13: Switching characteristics for the external clock mode