GP-22050

Data sheet

Revision 1.07 - February 2010

Table of Contents

Table of Tables

Table of Figures

References

[1] 8PI *Control Panel User's Guide* for GP-22050 (ug_GP22050_8PIControlPanel.doc)

[2] TCL scripting for ADWG application (ug_GP22050_ADWGTclLib.pdf)
This document explain how to control the GP22050 using the Tcl scripting interface. It also contains a complete list of all available procedures to operate in ADWG mode.

[3] C/C++ library for ADWG application (ug_GP22050_ADWGCLib.pdf)
This document describes the different functions available in the C/C++ library provided with the ADWG application.

[4] TCL scripting for Analyser application (ug_GP22050_AnalyserTclLib.pdf)
This document explain how to control the GP22050 using the Tcl scripting interface. It also contains a complete list of all available procedures to operate in Analyser mode.

[5] C/C++ library for Analyser application (ug_GP22050_AnalyserCLib.pdf)
This document describes the different functions available in the C/C++ library provided with the Analyser application.

[6] TCL scripting for Analyser application (ug_GP22050_JTAGTclLib.pdf)
This document explain how to control the GP22050 using the Tcl scripting interface. It also contains a complete list of all available procedures to operate in Analyser mode.

[7] C/C++ library for Analyser application (ug_GP22050_JTAGCLib.pdf)
This document describes the different functions available in the C/C++ library provided with the Analyser application.

[8] TCL scripting for Analyser application (ug_GP22050_SVFTclLib.pdf)
This document explain how to control the GP22050 using the Tcl scripting interface. It also contains a complete list of all available procedures to operate in Analyser mode.

[9] C/C++ library for Analyser application (ug_GP22050_SVFCLib.pdf)
This document describes the different functions available in the C/C++ library provided with the Analyser application.

Revision history

Version	Date	Description
1.00	May 2005	Preliminary version
1.01	Sept 2005	Reviewed
1.01b	January 2006	Updated continuous throughput figures
1.02	June 2006	Limited software presentation / Reviewed
1.03	July 2006	Update of DC and AC characteristics
1.04	November 2006	Reviewed / Renewed for software version 1.04
1.05	August 2007	Added pattern depth limitation
1.06	August 2009	Added HW revision changes
1.07	February 2010	I2C port description update

1 Features

- High-speed USB 2.0 host interface (full-speed 12 Mbps and high-speed 480 Mbps)
- Configurable system interface: up to 16 bidirectional data and 6 bidirectional control signals
- System interface local frequency up to 50 MHz
- Maximum burst throughput: 100 MByte/s
- Maximum continuous throughput: 48 MByte/s[1]
- Indicative actual continuous throughput: 11 MByte/s[2]
- 16 kB internal memory buffer
- 'On-the-fly operation' – allowing up to 100 MByte total depth / run
- Selectable internal (USB bus) or external power supply for I/Os voltages
- System interface operating from +1.2V to +3.3V (extensible with plug-in hardware modules).
- Delivered with the 8PI Control Panel software suite, including: documentation, drivers and upgradeable host control software
- Provides multiple and flexible bidirectional access points to a system-on-board under test.
- Applications[3]:
  - JTAG (IEEE 1149.1) access;
  - Logic analyser;
  - ADWG (Arbitrary Digital Waveform Generator) / pattern generator;
  - Board access through serial protocols: SPI, I²C, I²S, RS232, …
  - 8 bits/16 bits microcontroller interface;
  - Bus master / slave emulation;
  - SRAM, flash interface;
  - System debug and system prototype access;
  - IP evaluation;
  - Recorder/player tools.

2 GP-22050 Overview

Byte Paradigm GP-22050 (Figure 1) is a high-speed programmable bidirectional interface that allows the stimulation and the analysis of digital electronic systems.

Connected to a PC through a USB 2.0 interface and using a fully programmable hardware accelerator, the GP-22050 enables a flexible and powerful access to electronic system boards and electronic devices under test.

Figure 1: GP-22050

The GP-22050 is able to generate virtually any serial or parallel protocol that fits in 16

[1] The limiting factor is the host computer controlling the GP-22050. 48 MByte/s is the maximum throughput achievable by the USB 2.0 connection hardware implementation.
[2] Informative only – depends on the host PC. Result of a test with the ADWG application with a Pentium 4 3 GHz host computer.
[3] Each application requires proper mode of operation. Please contact Byte Paradigm to check about modes of operation roadmap and availability.

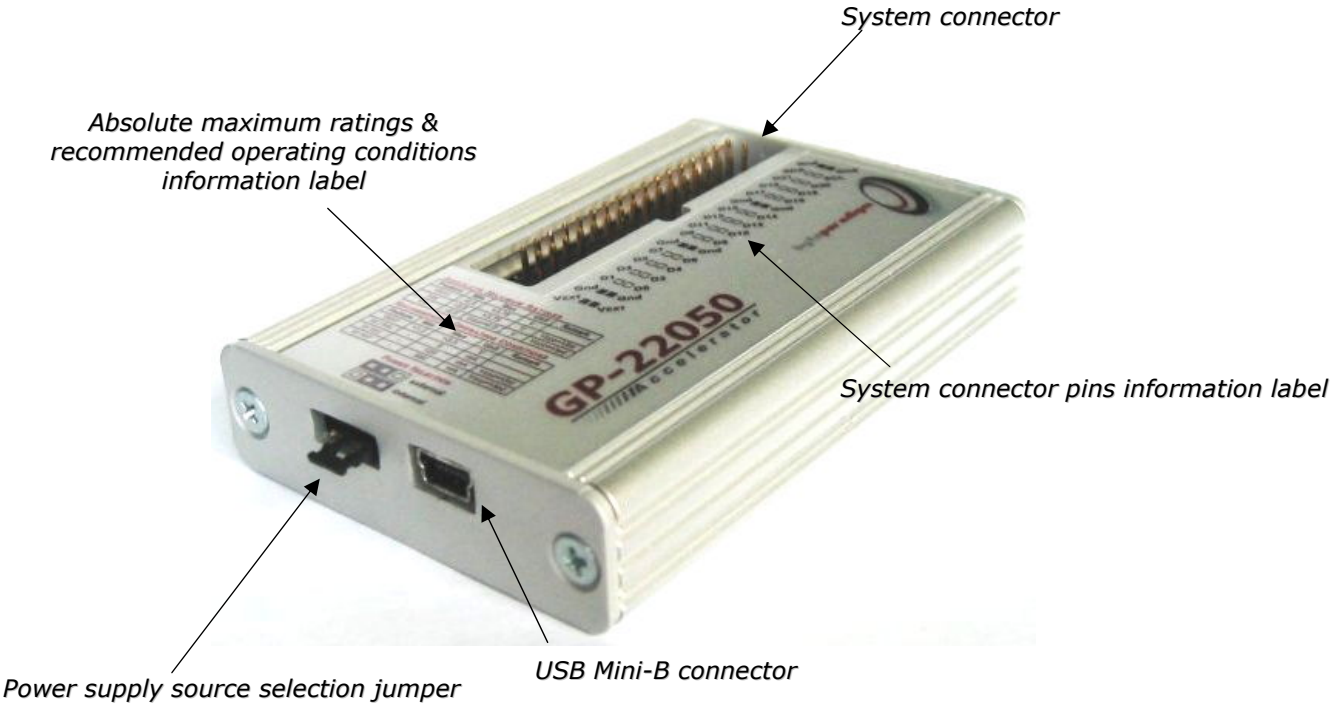
address/data lines and 6 control lines, up to 50 MHz (100 MByte/s burst performance). During operation, the hardware accelerator reduces the control flow to a minimum to reserve the bandwidth for data transfer. The GP-22050 is able to sustain a theorical continuous throughput of 48 MByte/s[4]. The actual throughput for continuous transfer depends on the host PC performances and can be expected at 11 MByte/s[5]. For most usages – and only for 3.3V I/O standards – the GP-22050 is powered directly through the host PC USB connection, enabling a very quick device setup. Additionally, an external power supply can be connected to the GP-22050 Accelerator device when higher current must be sinked through the system or when another I/O voltage is required.

3 Connecting the GP-22050

3.1 GP-22050 at a glance

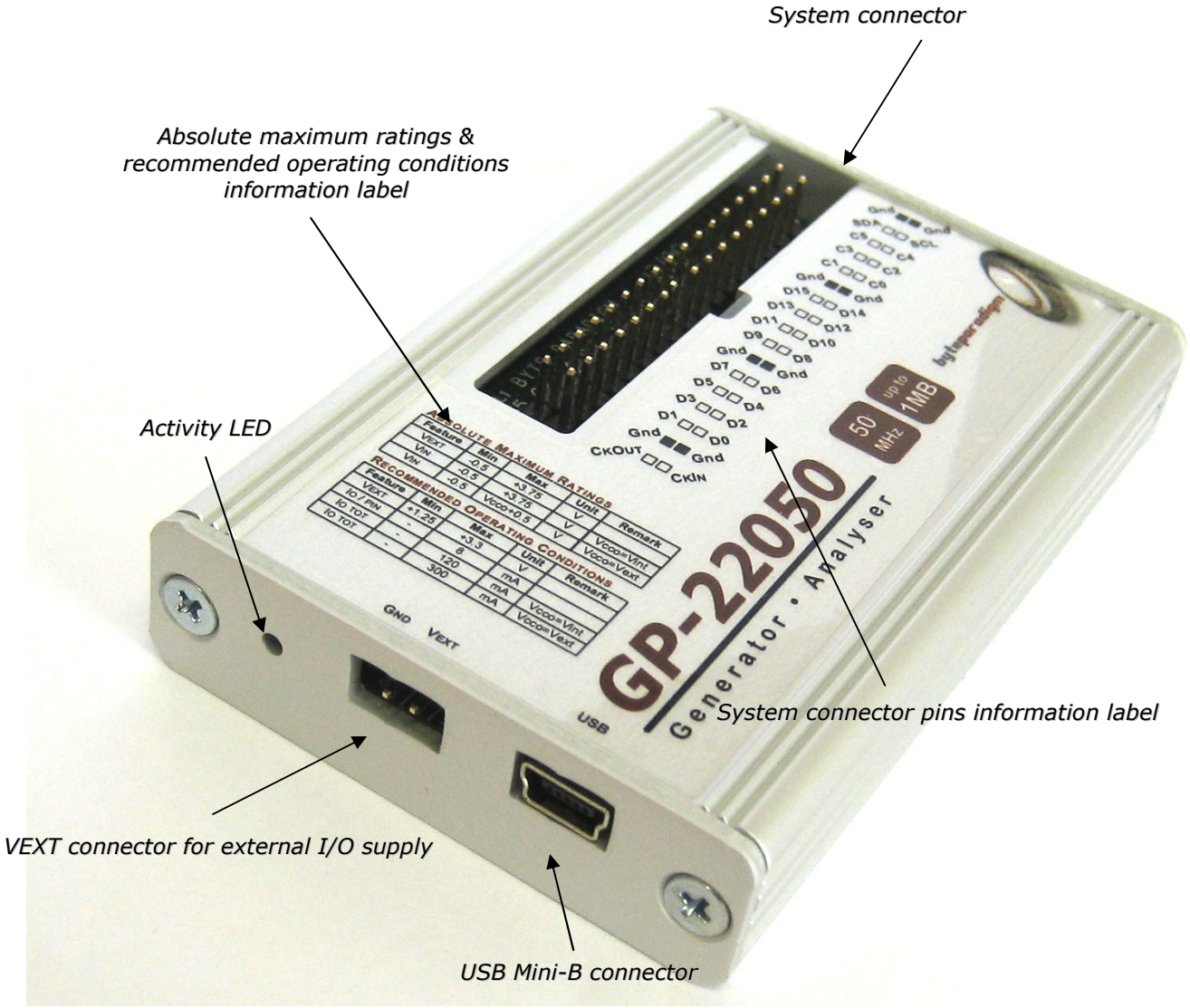
Several hardware revisions of the GP-22050 exist. Please first check the serial number located at the back of the device, with a barcode. The 2 first digits are the hardware revision number. It can be 01, 02 or 03. According to the hardware revision, the device features are slightly different.

Figure 2: GP-22050 Accelerator overview – HW revision 01



[4] Actually, the USB 2.0 high speed connection throughput is 60 MB/s (480 Mb/s); this bandwidth must be shared between the data and the USB protocol controls.
[5] Result of a performance test with a Pentium 4 3GHz PC, GP-22050 configured as a pattern generator.

Figure 3: **GP-22050 Accelerator overview – HW revision 02**



3.2 Minimum Host PC requirements

The GP-22050 connects to any PC using Microsoft Windows 2000 or Windows XP operating systems through a USB 1.x or USB 2.0 port connector. To benefit from the GP-22050 performance abilities, it is however recommended to use a USB 2.0 port, high-speed mode (480 Mbps).

3.3 Operating power

The main power supply of the GP-22050 is taken from the USB bus to provide the necessary voltage to the device core. The system interface can be powered either from the USB bus (internal power supply mode), either from an external power supply.

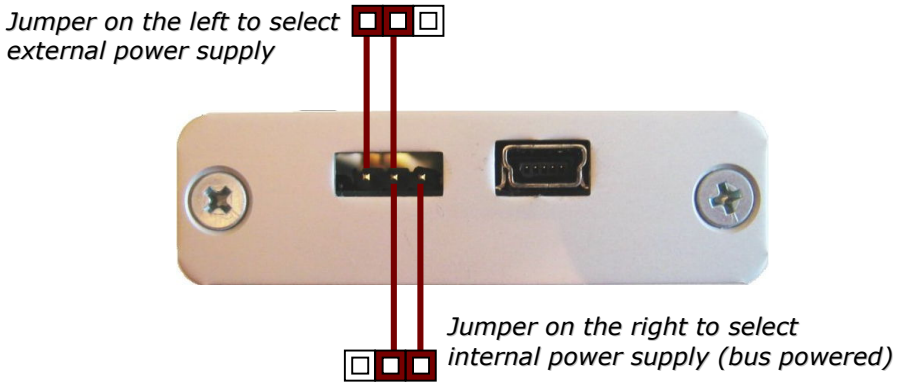
When the internal power supply mode is selected, the GP-22050 is then fully bus powered and operates without any external power supply. In this mode, the voltage level of the system interface is fixed to +3.3V (Refer to section "4 DC and Switching Characteristics" for more details on the compatible I/O voltage levels for the system connector).

The system connector can however operate at different voltage level between +1.8V and +3.3V. To enable this mode, an external power supply must be applied to the system connector V_{EXT} pins and the external supply mode must be selected.

For Hardware revision starting with 01

A ***power supply source selection jumper*** is located at the side of the GP-22050, on the left of the Mini-B USB connector. When the two left pins of the connector are shorted, the external mode is selected and an external power supply has to be provided by the user (Refer to Figure 4). When the two right pins are shorted, the internal mode is selected.

Figure 4: GP-22050 power source selection for HW revision 01



To switch the power supply mode the following sequences must be respected.

Enabling the external power mode:

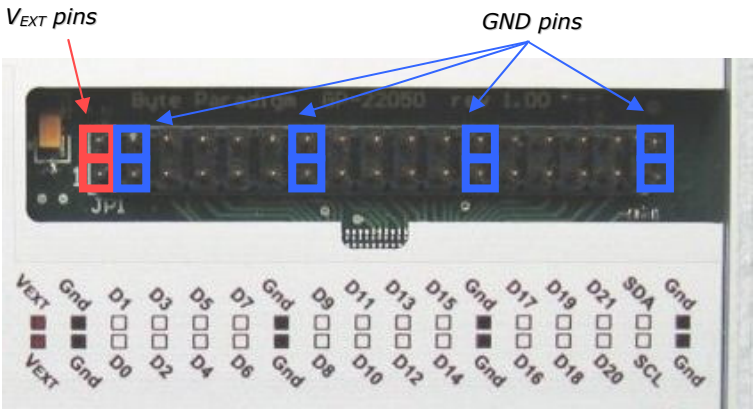
1. Disconnect the device from the USB bus
2. Change the jumper position to select the external mode
3. Connect the system interface GND pins of the system interface to the reference of the external power supply.
4. Connect and apply the external power supply to the V_{EXT} pins of the system connector.
5. Connect the device to the USB bus.

Enabling the internal power mode (bus powered):

1. Disconnect the device from the USB bus
2. Shut down and disconnect the external power supply.
3. Change the jumper position to select the internal mode
4. Connect the device to the USB bus.

To improve signal integrity it is recommended to connect as many GND pins as possible to the reference ground of the system under test.

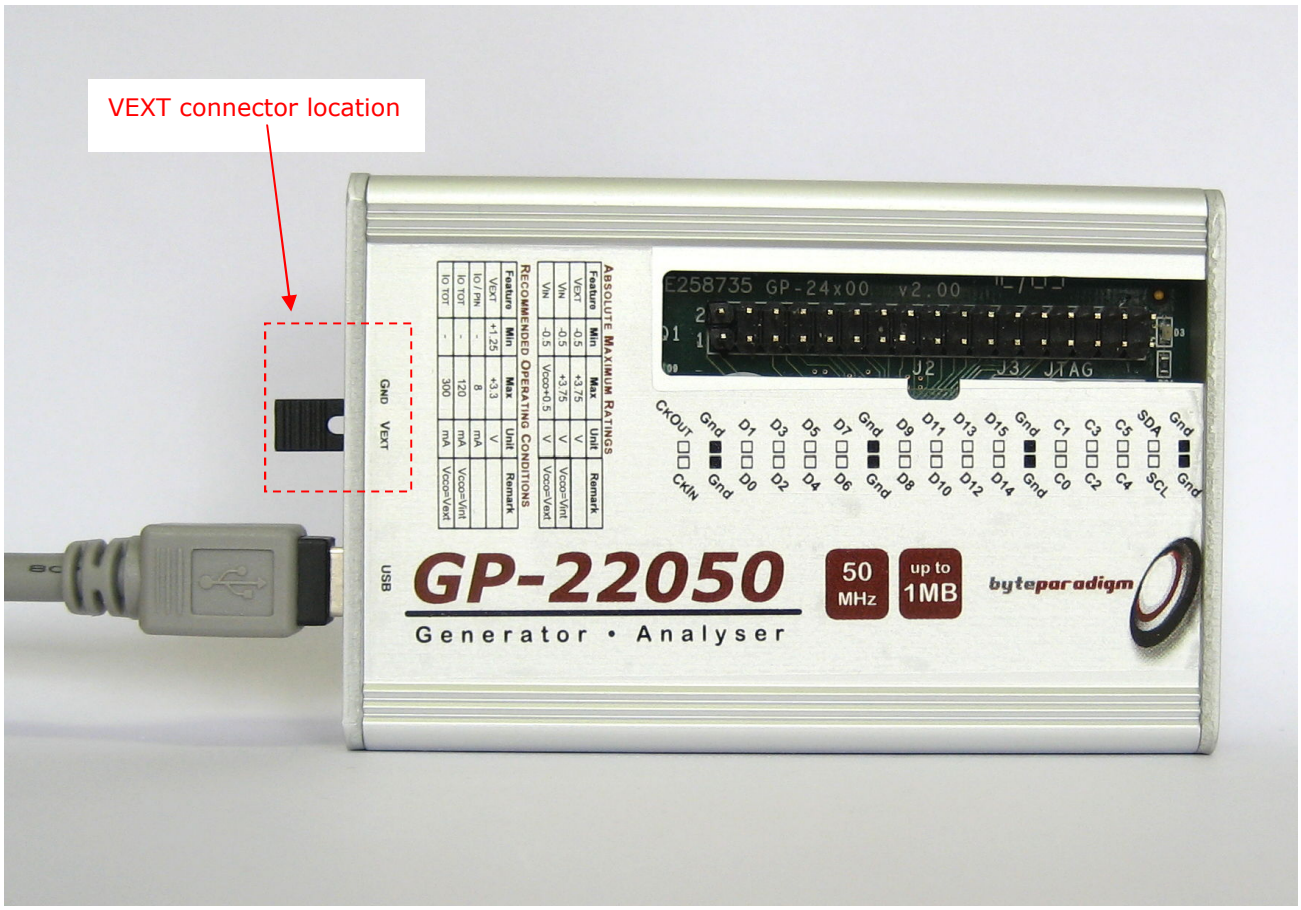
Figure 5: System connector external power supply pins for HW revision 01

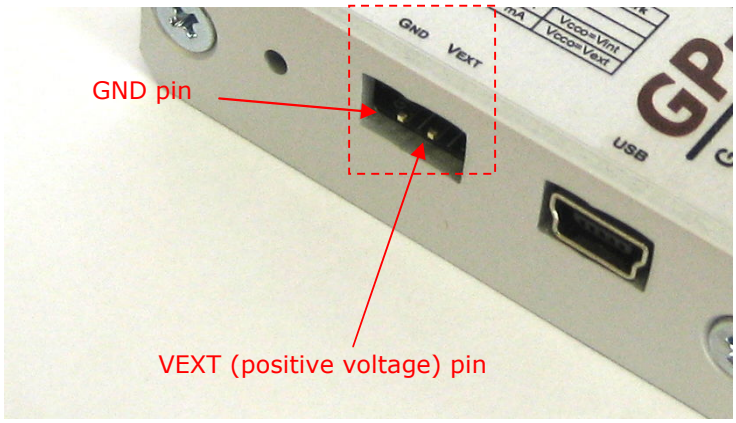


For Hardware revision starting with 02 or 03

An external power supply connector is located at the side of the device. It is protected with a jumper. This power connector is labelled "GND VEXT". **! Respect the connector polarity when using !**

Figure 6: System connector external power supply pins for HW revision 02 or 03





Enabling the external power mode:

1. Disconnect the device from the USB bus
2. Remove the jumper from the VEXT connector
3. Connect and apply the external power supply to the V_{EXT} pins of the system connector.
4. Connect the device to the USB bus.

Enabling the internal power mode (bus powered):

1. Disconnect the device from the USB bus
2. Shut down and disconnect the external power supply.
3. Connect the device to the USB bus.

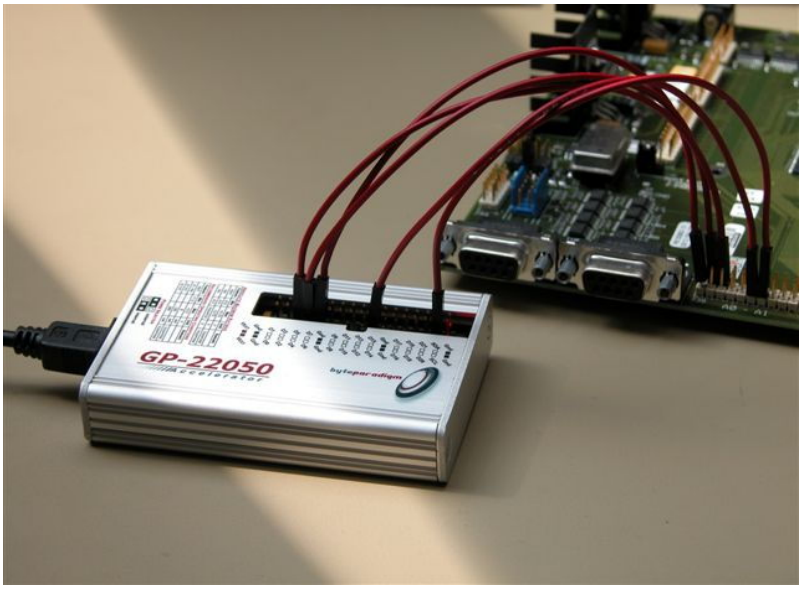
3.4 USB and system interface connections

Figure 7: USB mini-B to USB type A cable

A 2 meters USB mini-B to USB type A is provided with all GP-22050 packages (Figure 7).

A set of 34 flying lead wires connect the GP-22050 to the board under test. A standard pin header with 2.54 mm (0.1 inch) pitch must be foreseen on the target board where access is desired (Figure 8). A standard 34 way F-F flat cable (delivered as option) can also be used but offers less flexibility for pin mapping and for the connection of multiple board access points.

Figure 8: GP-22050 Accelerator connected with flying lead wires



3.5 Hardware accelerator configuration

The GP-22050 hardware accelerator device embeds several dedicated hardware processing units to guarantee signal timing accuracy and overall throughput. A GP-22050 hardware/software system is **application-oriented.** The GP-22050 available commands depend on the selected mode of operation. The hardware accelerator parameters are updated 'on-the-fly' by the *8PI Control Panel* software to ensure optimal performance for each application, according to a 'Same hardware / Multiple mode' principle.

3.6 Hot plug and play

The GP-22050 USB device can be attached and removed from the host computer without having to power-down or reboot. There is a delay after connecting the device to the host system before it is actually functional and reported as one of the Windows devices; during this time, the host software detects the GP-22050 and programs its hardware settings.

3.7 Flexible system interface

Features:

- Up to **16 data lines** and **6 control lines**;
- **Individual pin direction configuration**: input, output, bidirectional;
- **Individual functional signal allocation** onto the system connector;
- **Internal or external clocking reference** - 1 specific control input for external clocking;
- Dedicated SDA and SCL signals lines with pull-ups for **I²C bus control.**

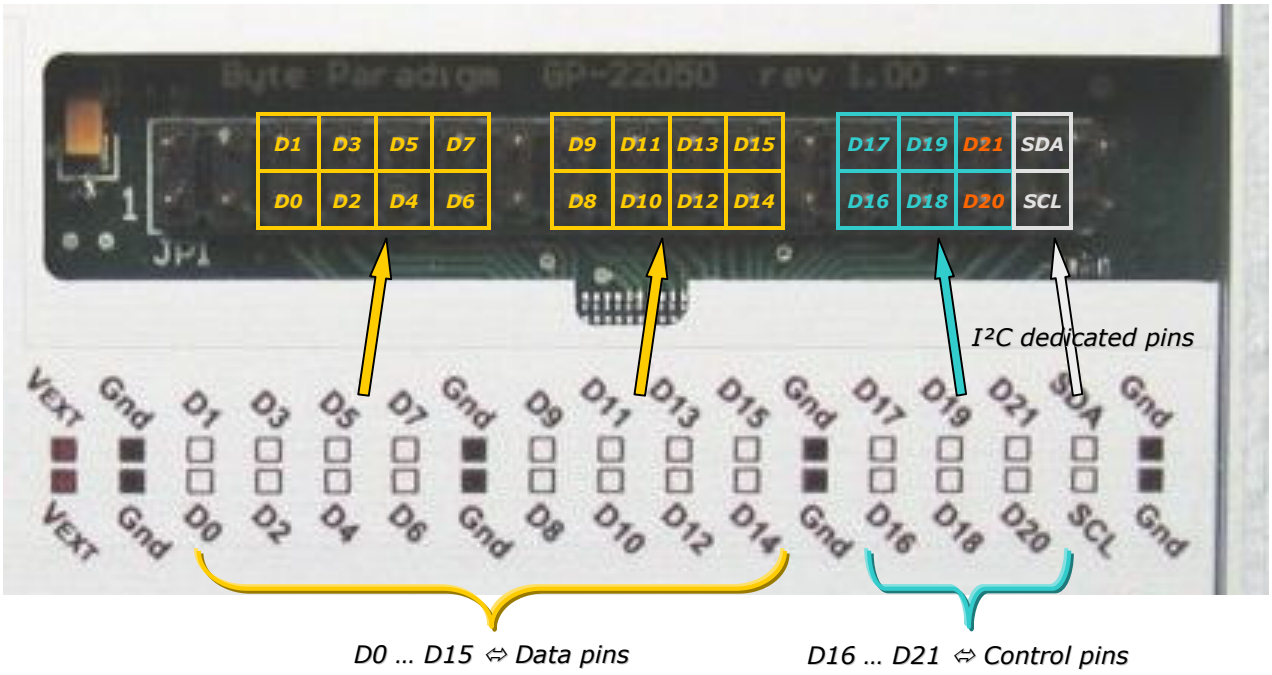
3.7.1 Data / Control partition, allocation and configuration

The **system interface** connects the GP-22050 Accelerator to the electronic system under test (Figure 8). For that purpose, a set of flying leads wires ensure the link between the system under test and the GP-22050 **system connector**. Using flying leads wires offer a 'physical flexibility' for GP22050/system signal mapping.

For hardware revision 01

As depicted on Figure 9, the system connector pins are grouped as **data pins** and **control pins.** The SDA and SCL pins are special control pins used for I²C bus control.

Figure 9: System connector pin groups allocation for HW revision 01

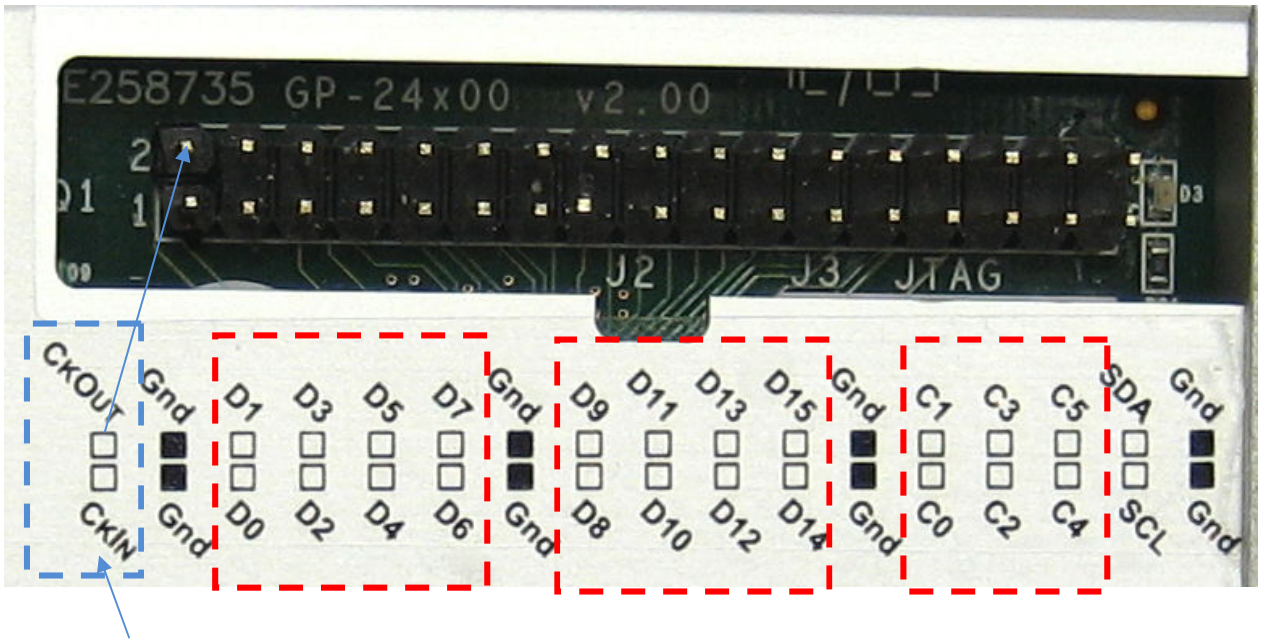


Besides these 2 groups, the other pins are voltage and GND pins and cannot be used for functional signalling (refer to section 3.3).

- **Data pins:** system connector pins labelled from **D0 to D15**.
- **Control pins:** system connector pins labelled from D16 to D21. Moreover, some control pins have a dedicated use for input and output clock signals, when used:
  - **output clock signal** is mapped onto the **D21** control pin.
  - **input reference clock signal** must be mapped onto the **D20** control pin.
- **I²C pins:** SDA and SCL are specific control pins for I²C bus interfacing.

For hardware revision 02 or 03

Figure 10: System connector pin groups allocation for HW revision 02 or 03



During GP-22050 operation, a set of functional signals are defined to access the system under test, according to the chosen application. These signals must be considered either as data signals or as control signals. **Within each group** (data or controls), the connector pins can be reserved for any functional signal defined to access the system under test. Each pin/signal can be individually defined as an **input,** an **output** or a **bidirectional**. Control and data signals are defined according to their purpose within a given access protocol and the possibility to update/visualise them through the host software; their respective characteristics are summarised in Table 1.

Table 1: Control / Data signals definition

Signal type	Direction	Description / Usage
Control	Output	The user can define one or several repetitive output control sequences managed autonomously by the GP-22050 Accelerator. For example, output control sequences are used for repetitive signal sequences for which timing is critical.
Control	Input	The user can define one or several input control sequences used as event to trigger an autonomous response from the GP-22050. The history of the inputs on the control lines cannot be collected by the host computer through the USB 2.0 connection. For example, input control sequences are used as start trigger to collect data (on the data pins) and send them to the host computer.
Control	Bidir	These sequences combine the 2 above types of control sequences.
Data	Output	The data sent to the GP-22050 system connector are defined and updated by the user through the host software. Repetitive sets of data can be defined as well and memorised in the GP-22050 Accelerator embedded memory.
Data	Input	Input data are sampled on the system connector and forwarded all along the GP-22050 data path to the user through the USB 2.0 interface and the host software.
Data	Bidir	Bidirectional data signals are defined for protocols where data must be sampled and sent over the same physical lines.

A given mode of operation can restrict the system interface flexibility to the configuration options strictly required for it. For example, the JTAG application package restricts signal definitions to TDI, TMS, TCK and TDO. TDI, TMS, and TCK are fixed as outputs; TDO is the only input.

3.7.2 System interface clocks

Two optional clock signals can be mapped onto the system connector:

- An **input clock signal**: this clock signal comes from the system under test and is used as the reference clock signal to generate and sample data and controls onto the system connector. If this clock signal is used, it must be mapped onto:
  - the system connector **D20** control pin **if the hardware revision is 01**;
  - the **CKIN pin if the hardware revision is 02 or 03.** Alternatively, if no external reference clock signal is provided, the GP-22050 internal clock signal is used.
- An **output clock signal**: when a clock reference has to be provided to the system under test by the GP-22050, this signal is conventionally mapped onto:
  - the system connector **D21** pin **if the hardware revision is 01;**
  - **the CKOUT pin if the hardware revision is 02 or 03.**

The GP-22050 Accelerator clock frequencies are defined through the host software. Table 2 summarises the available frequency ranges, and how to set them.

Table 2: System interface clocks frequency ranges

Clock	Frequency range	Description / Options
External reference clock	F_{EXT} / 2^{16} to F_{EXT} ; F_{EXT} max = 50 MHz	
Internal reference clock	763 Hz to 50 MHz	The GP-22050 Accelerator contains a clock divider unit, programmable with a 16 bits register. If ClkDiv is the value of this register, the achieved clock frequency is: frefclk / (ClkDiv + 1)
Output clock (D21)	- to 50 MHz	

3.7.3 I²C bus control dedicated signal lines

The SDA and SCL pins are pulled-up with a resistor of **2.2kΩ**, for I²C protocol interfacing on hardware revision 01.

On hardware revisions 02 or 03, the pull-up resistors value is **4.7 kΩ**.

Alternatively, the D1 (for SDA) and D0 (for SCL) can be used for I2C master / analyzer. These pins do not feature any pull-up resistor. Please refer to the 8PI Control Panel user's guide for more information on how to activate this alternative port (this feature is available from 8PI Control Panel version 1.08f).

3.7.4 System interface performance

The maximum clock rate for the system connector signals is 50 MHz. When all the system interface signals are configured with the same I/O direction, the maximum achievable throughput is: 16 bits x 50 MHz = 800 Mbps, that is to say **100 MByte/s.**

It is important to note that this throughput can be sustained as long as sufficient data are available. As described at section 3.8.2, this mainly depends on the local buffering memory available for the data transfer. Up to 16 kB memory can be allocated. However, because the GP-22050 performs 'on-the-fly' data transfer to/from the host PC, the total data depth available is in reality limited 100 MByte, if the data transfer rate is held below a PC-dependant level. The 'continuous throughput' is an indicative figure mentionned with the GP-22050 performance figures. It is the maximum sustainable throughput for 'infinite' data transmission to and from the host PC. Tests conducted on a Pentium 4, 3GHz PC show sustainable throughput up to 11 MByte/s.

3.8 Hardware accelerator processing unit

Features:

- High performance real-time (cycle accurate) processor.
- Local memory for data buffering.
- Data compression for optimised USB bandwidth use.

3.8.1 Optimised protocol implementation

To access a system under test, the GP-22050 implements cycle-accurate protocols onto its system interface. Despite for low-performance protocols (low bandwidth needs), a hardware acceleration is compulsory to guarantee protocol timings at clock rates up to 50 MHz. This section summarises the HW/SW partition and relationships of the GP-22050.

The GP-22050 hardware processing is based on a specialised high-performance real-time processor[6]; its main functionalities are summarised hereafter.

- Generate arbitrary and repetitive cycle-accurate sequences on the control lines.
- Trigger responses upon detection of arbitrary sequences on the control lines (the data lines can be used as well for some application packages).
- Synchronise incoming and outgoing data with the control signals, according to the used application/protocol.
- Generate the clock signals.

Functionally, the GP-22050 real-time processing unit can be seen as a general-purpose hardware resource for the implementation of a finite state machine (FSM), optimised to the performance needs of a given application/protocol. When the user switches from an application to another one on the 8PI ControlPanel host software, the GP-22050 processing unit selects a new FSM, best suited to the new application/protocol. This mechanism guarantees an automatic synchronisation between the host computer running a validation/analysis application and the hardware acceleration resources required to run it (Figure 11).

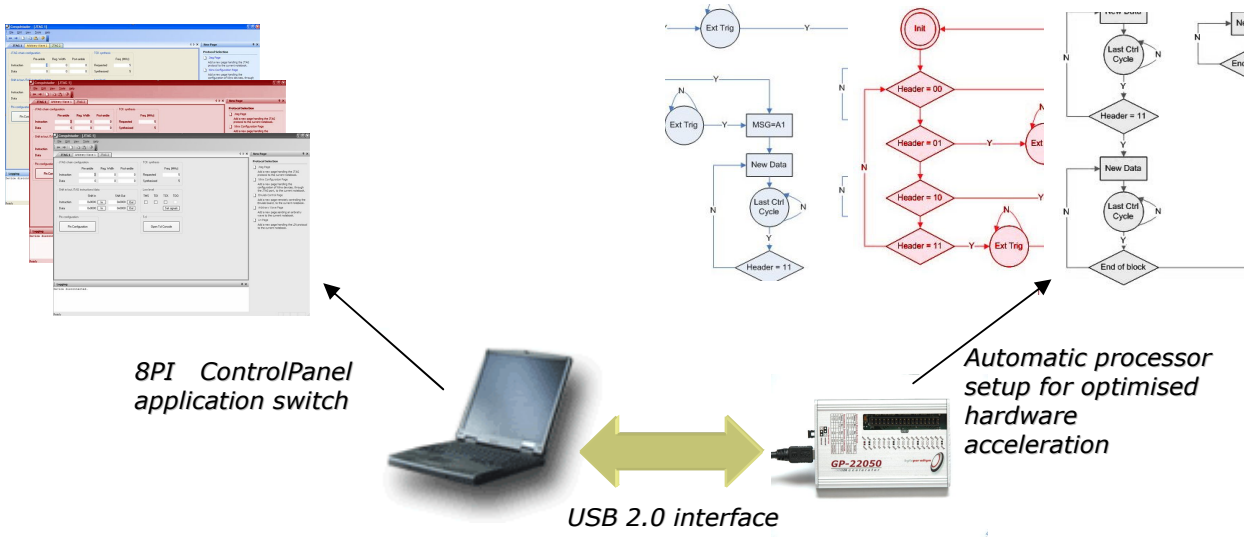


Figure 11: GP-22050 automatic application / hardware acceleration synchronisation

3.8.2 Adaptable local data buffering

The GP-22050 hardware processing unit uses a memory buffer of 16kB[7] to locally store host controls and data and ensure efficient data transfers.

[6] Proprietary of Byte Paradigm.
[7] 16 kB memory available in standard. Please contact Byte Paradigm for other memory amounts.

From the host PC to the system under test, the data transits through the USB interface; it is then buffered in local memory by the GP-22050 Accelerator processing unit and sent the system connector through the system interface. From the system under test to the host, the path is just backwards: from the system connector through the system interface and the processing unit to the local memory buffer, and from the memory buffer to the host through the USB interface (Figure 12 & Figure 13).

Figure 12: Default transmission data path

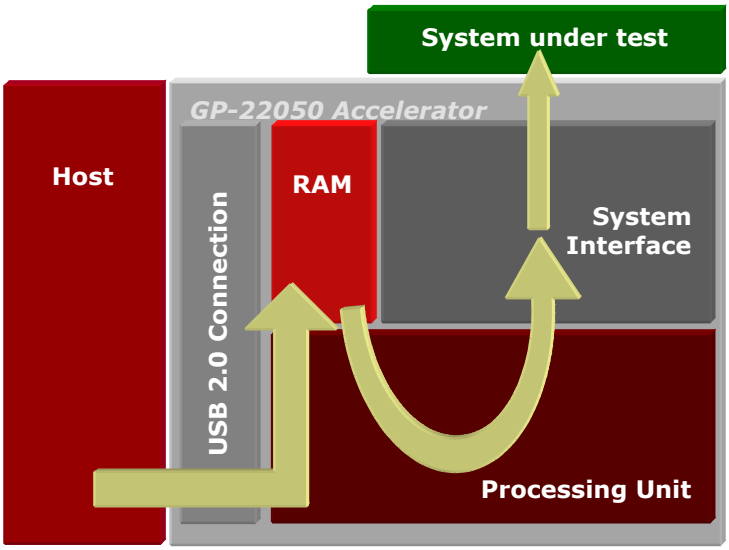
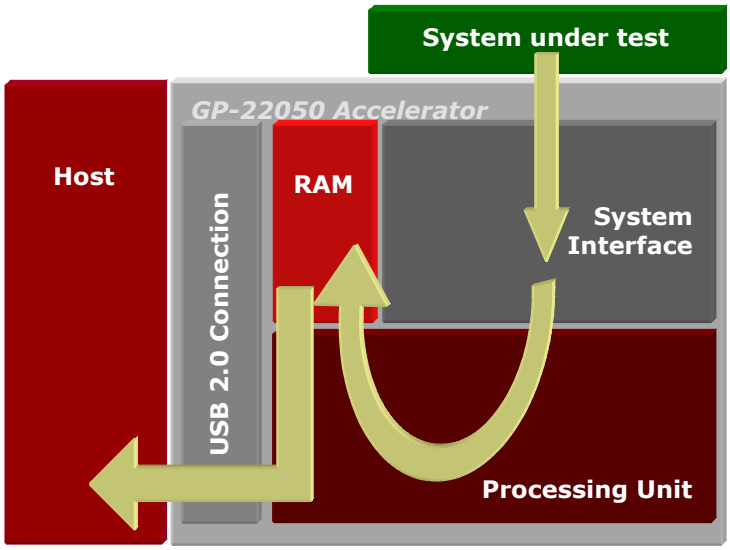


Figure 13: Default reception data path

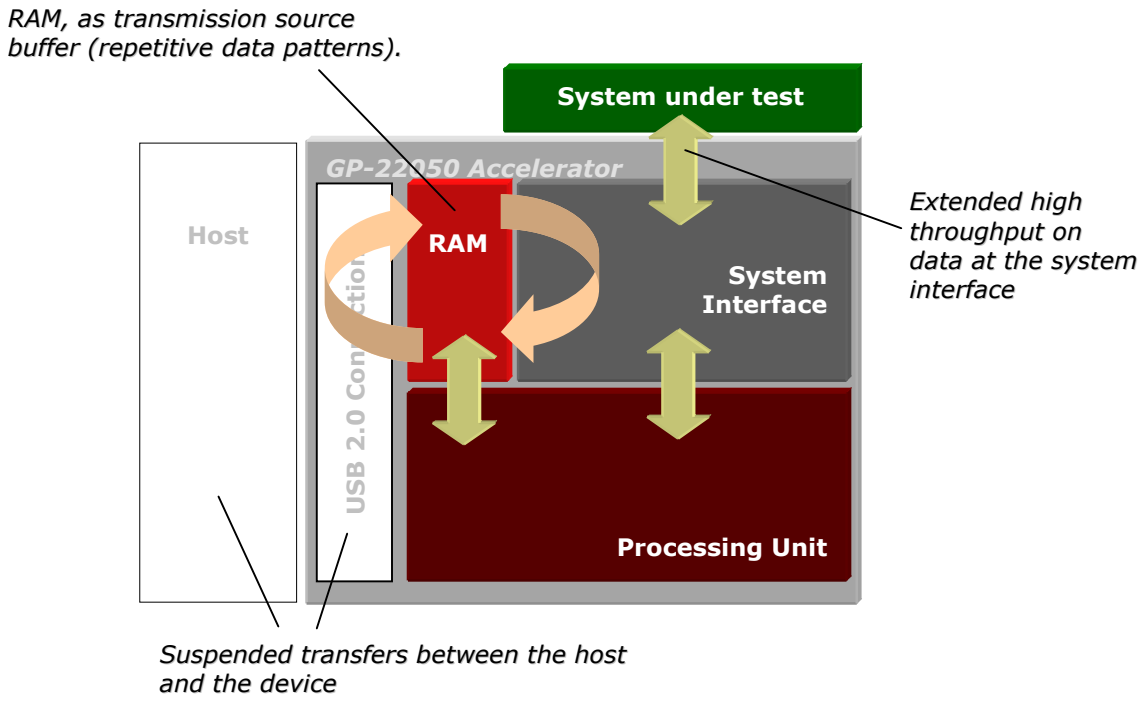


At the system interface, the GP-22050 Accelerator is able to sustain the maximum throughput speed (16 bits data @ 50 MHz) for a burst length equivalent to the allocated local memory buffer. Attempting to go over this burst length at maximum 50 MHz speed will result in data underflow (transmission) or overflow (reception) because the USB 2.0 connection will not be able to provide/collect the data at that rate. The USB connection with the host PC is managed by the 8PI Control Panel software. It is important to note

that the transfers between the GP-22050 and the host PC occur as soon as data is available (on-the-fly operation). As a result, the maximum throughput that is actually achievable over an amount of data that exceeds the embedded 16 kB is limited by the PC ability to collect or send data over the USB link at a sufficient rate. Tests performed on a Pentium 4 3GHz PC show sustainable throughputs up to 11 MByte/s[8].

However, in some specific cases, the GP-22050 Accelerator can be set in infinite loop / repeat mode (Figure 14). In this mode, the data transfer from/to the host can be suspended and the processing unit can then operate at full speed over a longer set of data. For example, this would be the case if data sequences must be repeated on the system connector. The maximum length of the repeated data set is limited to the 16 kB device memory. This specific mode of operation is made available according to the mode of operation used. Please refer to software user guide for more information about how to control this mode.

Figure 14: GP-22050 infinite loop / repeat mode



The total memory space can be freely partitioned between data transmission and data reception operations, according to the application needs. This setting is part of the processing unit configuration.

3.8.3 Efficient bandwidth use

To benefit from the USB 2.0 high speed connection while allowing a configurable data word width (on the system interface, the data word width can be configured from 1 to 16 bits, in power of 2 steps) a data compression/decompression is performed at the transmission of data between the GP-22050 processing unit and the USB 2.0 interface.

[8] Informative only

4 DC and Switching Characteristics

4.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Description	Conditions	Min	Max	Unit
V_{EXT}	External DC supply voltage relative to GND		-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{INT}	-0.5	+3.75	V
V_{IN}	Voltage applied to any user I/O pins relative to GND	V_{CCO}[2] = V_{EXT}	-0.5	V_{CCO}+0.5	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to V_{INT} or V_{EXT} when, respectively, the internal or external supply source is selected (refer to section 3.3 for more details on the powering scheme).

4.2 Recommended operating conditions

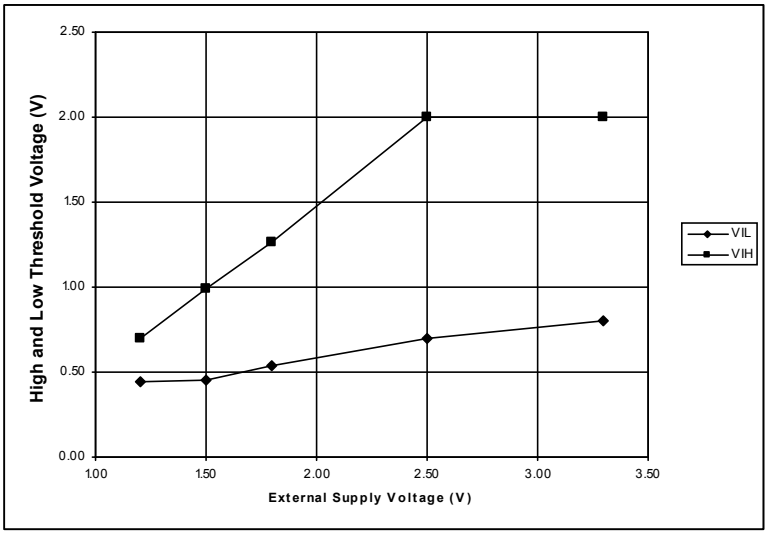
Table 4: Recommended operating conditions

Symbol	Description		Min		Max	Unit
V_{EXT}	External DC supply voltage relative to GND		+1.8	-	+3.3	V
I_{CCO}	Quiescent supply current for any user I/O pin.		-	-	8	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{INT}	-	-	120	mA
$I_{CCO-TOT}$	Total quiescent current for all user I/O used simultaneously	V_{CCO}[1] = V_{EXT}	-	-	300	mA
T_{OP}	Operating ambient temperature		0	-	45	°C
V_{IH}[2]	Logic high voltage threshold	V_{CCO}[1] = V_{INT}	2.0	-	-	V
V_{IL}[2]	Logic low voltage threshold	V_{CCO}[1] = V_{INT}	-	-	0.8	V
Rpu	Pull-up resistors on SDA and SCL pins	Hardware revision 01	-	2.2	-	kΩ
Rpu	Pull-up resistors on SDA and SCL pins	Hardware revision 02 or 03	-	4.7	-	kΩ

Notes:

1. Vcco is the supply voltage of the I/O pin output driver. Depending on the position of the power selection jumper it is equal to VINT or VEXT when, respectively, the internal or external supply source is selected.
2. Refer to Figure 15 for the V_{IH} and V_{IL} threshold voltage when the external supply voltage is selected.

Figure 15: User I/O input threshold voltage vs external supply voltage



4.3 System Performance

Table 5: Data throughputs

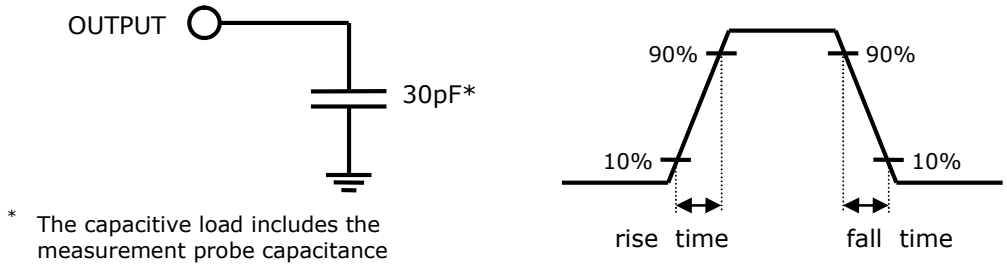
Description	Min	Typ.	Max	Unit
USB 2.0 interface total throughput	-	-	480 60	Mbps MByte/s
USB 2.0 interface throughput within GP-22050	-	-	48	MByte/s
User I/O operating frequency	-	-	50	MHz
System interface burst throughput[1]	-	-	100	MByte/s
System interface continuous throughput[2,3]	-	11	-	MByte/s

Notes:

1. The burst throughput is the performance achievable when performing transfers of 16 Kbytes or less.
2. The continuous throughput is the performance achievable when performing transfers of more than 16Kbytes. The throughput is dependent of the host computer performances. The provided values are given as indicative reachable performance only.
3. There is no limit in the maximum amount of data that can be transferred using the GP-22050. Continuous mode is then used to describe transfers larger than the internal device memory. The 8PI Control Panel software delivered with the GP-22050 limits a single data run to 100 MByte.

4.4 Switching Characteristics

Figure 16: Tests conditions



* The capacitive load includes the measurement probe capacitance

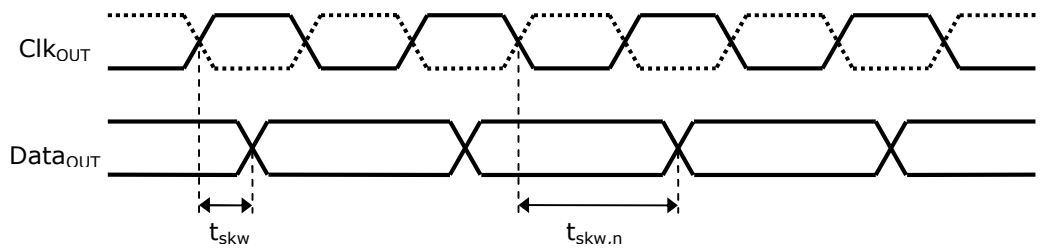
Table 6: Clock frequencies, rise and fall time, skews

Symbol	Description	Min	Typ	Max	Unit
F_{CLKI}	Internal clock frequency	763 Hz	-	50 MHz	
F_{CLKE}	External clock frequency	-	-	50	MHz
F_{CLKO}	Output clock frequency	-	-	50	MHz
t_{skw}[1]	Skew between clock out and the output lines when Clk_{OUT} is not inverted	-400	-50	300	ps
$t_{skw,n}$[1,2]	Skew between clock out and the output lines when Clk_{OUT} is inverted	T/2-400	T/2-50	T/2+300	ps
t_{lh}[3]	Output pin rise time	2.2	2.7	3.3	ns
t_{hl}[3]	Output pin fall time	4.4	5.4	6.6	ns

Notes:

1. The skew is measured taking Clk_{OUT} as reference (pin P21 on the user's interface connector). It represents the offset between the reference and all the other data output pins.
2. When Clk_{OUT} is inverted, the offset with the output data lines is incremented by T/2, with T equal to the output clock period.
3. Rise (10%-90%) and fall (90%-10%) time measured with internal supply voltage selected (+3.3V).

Figure 17: Skew between Clk_{OUT} and data output signals, with clock ratio equal to 1



4.4.1 Sampling Data Using the Internal Clock

The GP-22050 device can operates with an external reference clock signal provided by the user (applied on pin P20 of the system connector) or with the internally generated clock. Clk_{OUT} is the image of the internal clock. Clk_{INT} is the reference clock. All timing values in this section are measured from Clk_{INT} rising edge.

When the device is used in analyser mode, data can be sampled on Clk_{INT} rising or falling edge. The setup and hold time are measured relatively to the edge used to sample the data (refer to Figure 18).

Refer to [1] for more information on how to change the sampling edge and clock polarity.

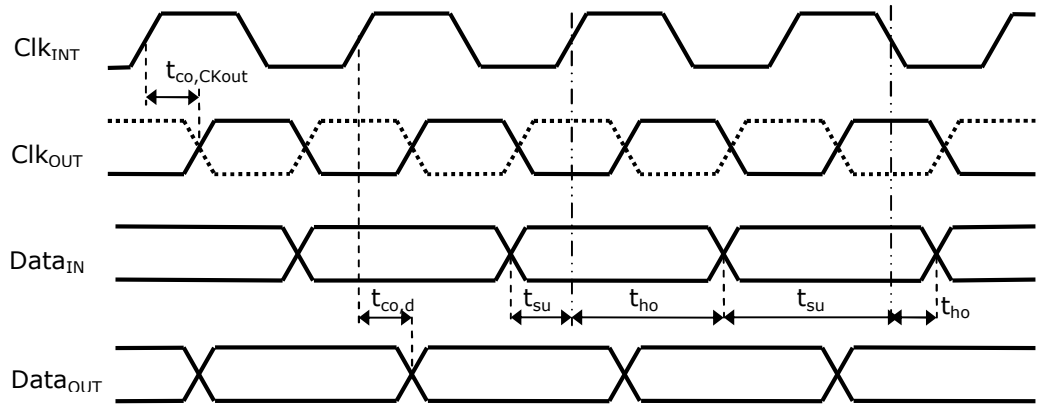
Table 7: Switching characteristics for the internal clock mode

Symbol	Description	Min	Max	Unit
$t_{co,CKout}$ [1]	Clock to output delay for signal Clk_{OUT}	2.0	6.0	ns
$t_{co,d}$ [1]	Clock to output delay for signal Clk_{OUT}	2.0	6.0	ns
t_{su} [2]	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho} [2]	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

Notes:

1. Values computed from used components manufacturer datasheet.
2. Setup and hold values are independent of the Clk_{INT} edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.

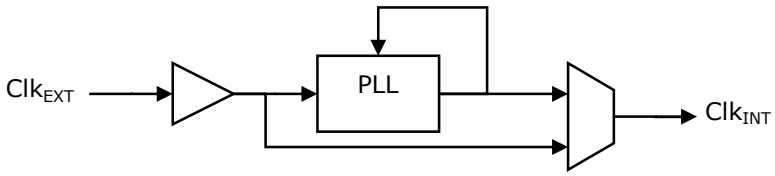
Figure 18: Switching characteristics for the internal clock



4.4.2 Sampling Data Using the External Clock

When the GP-22050 device operates in the external clock mode, the user supplied clock signal can follow two different clock paths to become the internal reference clock. One of the two paths includes a PLL to shorten the propagation delay. The internal clock is used as reference. All setup and hold values in this section are measured from the rising edge of to this clock Clk_{INT}.

Figure 19: Clock path from Clk_{EXT} to Clk_{INT}



When the device is used in analyser mode, data can be sampled on Clk_{INT} rising or falling edge. The setup and hold time are measured relatively to the edge used to sample the data (refer to Figure 20). When operating in arbitrary generator mode, all the outputs are generated on Clk_{INT} rising edge. Inverting the polarity of Clk_{OUT} does not change the edge used to send data out of the device.

Table 8: Switching characteristics for the external clock mode

Symbol	Description	Min	Max	Unit
$t_{co,CKout}$ [3]	Clock to output delay for signal Clk_{OUT} from reference clock $Clk_{INT.}$	2.0	6.0	ns
$t_{co,d}$ [3]	Clock to output delay for output data lines from reference clock Clk_{INT}	2.0	6.0	ns
t_{pce} [3]	Delay from Clk_{EXT} input pin to the internal reference clock Clk_{INT} when no PLL is inserted in the clock path.	2.7	8.4	ns
t_{pcep} [1,3]	Delay from Clk_{EXT} input pin to the internal reference clock Clk_{INT} when the PLL is inserted in the clock path.	1.8	4.5	ns
t_{su} [2]	Data setup time to internal reference clock for rising edge sampling mode.	-	1.6	ns
t_{ho} [2]	Data hold time from internal reference clock for rising edge sampling mode.	0.0	-	ns

Notes:

1. The PLL can only be used for clock frequencies greater than or equal to 20MHz (refer to [1] for more details).
2. Setup and hold values are independent of the Clk_{INT} edge used to sample the data. When the sampling edge is changed, the timing values remains constant, but the reference is change.
3. Values computed from used components manufacturer datasheet.

Figure 20: Switching characteristics for the external clock mode