Introducing SPI Xpress

SPI protocol Master / Analyzer on USB

SPI Xpress is Byte Paradigm's SPI protocol exerciser and analyzer. It is controlled from a PC through a USB 2.0 high speed interface. It allows debug, analysis, programming and testing of chips and electronic boards that use SPI for chip-to-chip communications.

It operates on standard SPI and many other serial protocol interfaces that slightly differ from the standard SPI protocol, including 3-wires interfaces with bidirectional data line, up to 50 Mbps data rate.

SPI Xpress is delivered with its control software (MS-Windows) including graphical user interface, waveform viewer, scripting TCL/tk interface and direct C/C++ DLL access.

This white paper introduces the unique features of the SPI Xpress Master / Analyzer.

Introduction to the SPI protocol

Overview

The Serial Peripheral Interface Bus or SPI is a synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slaves can be connected to a single Master and the 'classical' SPI standard is defined as a 4-wires interface including:

- SCLK - a clock signal generated by the master;
- MOSI - (Master Out Slave In) a master-to-slave(s) serial line;
- MISO – (Master In Slave Out) a slave(s)-to-master serial line;
- SS# - one or several slave select lines.

Figure 1 and Figure 2 show two typical SPI bus configurations.

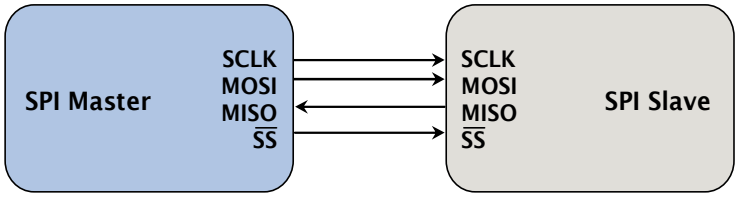

Figure 1 : Single master and single slave

Operation

The data exchange itself has no pre-defined protocol. To select a slave device,

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the master pulls the corresponding SS line low and starts transmitting data bits over the MOSI line synchronously to the generated SCLK. Simultaneously, the slave answers by shifting bits onto the MISO line.

Clock polarity and phase

The master always drives data on one edge of the SCLK clock onto the MOSI line and samples the incoming data from the MISO line on the alternate clock edge. When the slave select signal is not active, the clock is usually held at an IDLE level. The MOSI toggle edge, MISO sampling edge and the clock IDLE level are slave-device dependent. The SPI protocol defines 2 parameters, the **clock polarity** (CPOL) and the **clock phase** (CPHA); the possible combinations of these parameters are summarised as 'mode', conventionally numbered as described on Table 1.

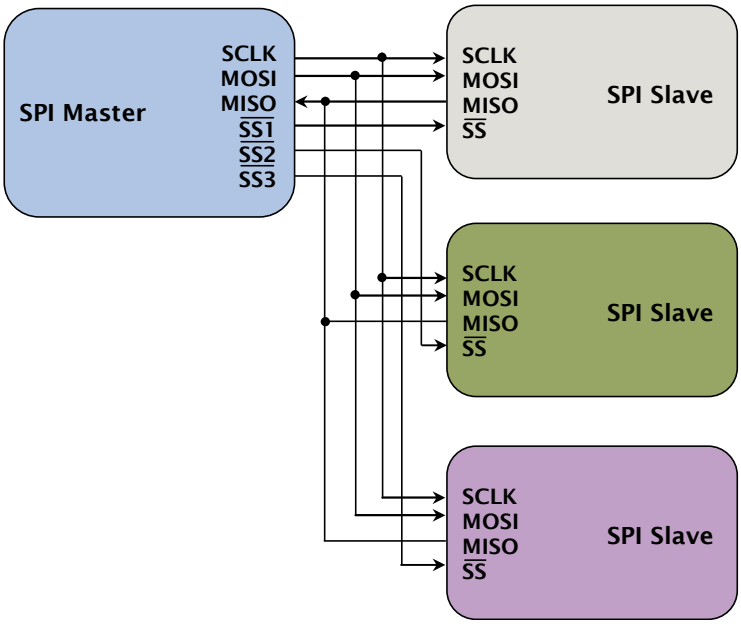


Figure 2 : Single master and three slaves

Many 'SPI-like' protocols

Because SPI is a kind of 'de facto standard', there is a wide variety of protocols defined on 4 wires, very similar to the standardised one. Some devices even have minor variances from the CPOL/CPHA modes described above. Devices often require extra clock idle time before the first clock or after the last one, or between a command and its response. Some don't use the conventional signal polarity (active low) for the SS lines; some require a defined minimum phase between the SS lines edges and the clock edges. Finally, some use a 3-wires signalling instead of the normal 4-wires one, using a single bidirectional MOSI/MISO line.

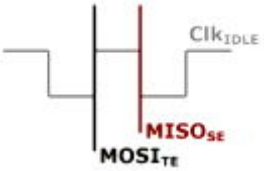
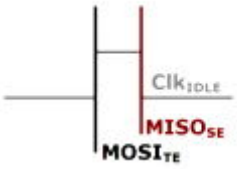
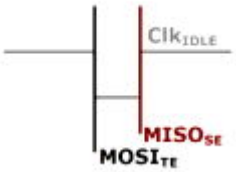
Mode 0 ***CPOL = 0*** ***CPHA = 0***		***Mode 2*** ***CPOL = 1*** ***CPHA = 0***	
Mode 1 CPOL = 0 CPHA = 1		**Mode 3** CPOL = 1 CPHA = 1	

Table 1 : SPI Modes

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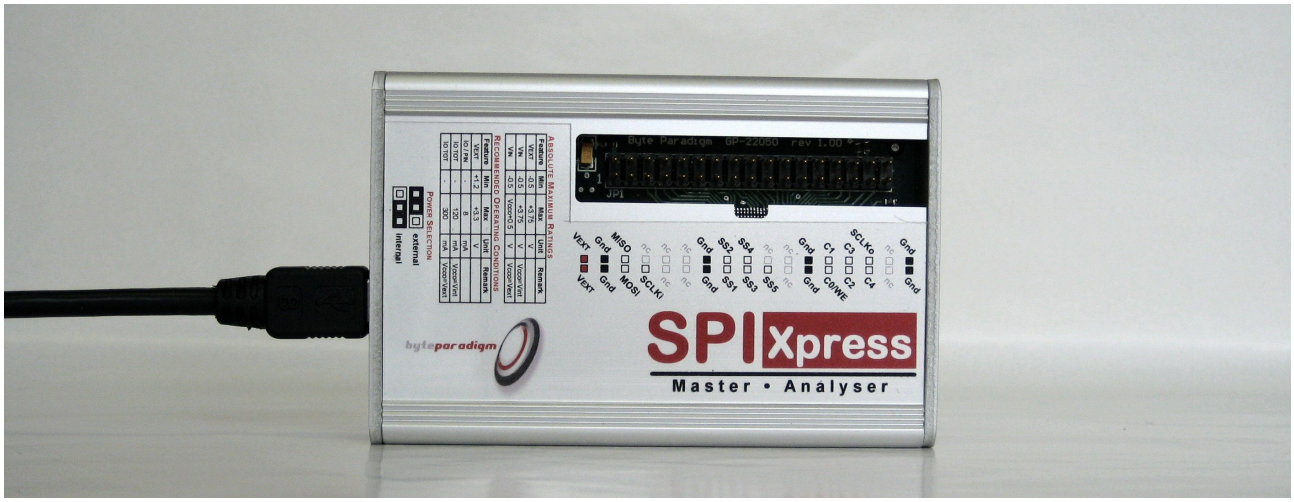
SPI Xpress – an advanced SPI and SPI-like protocol master and analyzer (SPI host adapter) in one USB 2.0 device.



Unique features and performance level

The following table compares SPI Xpress features with its nearest competitor.

	SPI Xpress	***Nearest Competitor***
Device type	**Master / Analyzer**	Master only
SCLK frequency range	**800 Hz to 50 MHz**	800 kHz to 40 MHz
SPI supported modes	All modes	All modes
Selectable SS polarity	YES	YES
Selectable bit ordering	YES	YES
Master operation log	YES	YES
Master operation recording	YES	YES
Master operation script execution	YES	YES
Non-continuous clock generation	YES	YES
Continuous clock generation	**YES**	NO
GUI	YES	YES
Free API	YES	YES
Integrated scripting	**TCL/tk**	NO
Configuration save	**YES**	NO
Number of slaves	**5**	3
Selectable SS edge position step	**¼ TSCLK up to 12.5 MHz** **½ TSCLK up to 25 MHz**	NO
SS# assertion / de-assertion to/from first clock edge	**0 x T_{SCLK}** **(no latency)**	at least 1 x T_{SCLK}
3-wires protocols support	**YES**	NO
Separately selectable length for write, write-to-read latency and read (3-wires interfaces)	**YES**	n.a.
Bus direction output	**YES**	n.a.
Optional external trigger	**YES**	n.a.
Trigger pattern width	**Up to 6 bits**	n.a.
Selectable edge/level trigger	**YES**	n.a.
Analyzer trigger positioning	**YES**	n.a.
Integrated waveform viewer	**YES**	n.a.
Selectable analyzer decoding format	**YES : raw data, raw SPI data, decoded SPI**	n.a.

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SPI Xpress fits to SPI and many other 4- and 3- wires serial protocols

SPI Master protocol interfaces (SPI host adapter)

SPI Xpress Master operation is based on the standard 4-wires SPI protocol. SPI Xpress Master combines the flexibility of a USB PC-controlled instrument with a dedicated hardware to access SPI ports as a master. The basic SPI protocol parameters are:

- SCLK frequency;
- SPI Mode (clock polarity and clock phase);
- Transaction length;
- Number of slaves.

More advanced parameters include SS# signals polarity, transaction bit ordering, continuous / interrupted (hole) clock generation and so on.

SPI protocol parameters are set up from the host PC running 8PI Control Panel software and downloaded into the SPI Xpress device through the USB link. During transfers, MOSI/MISO data bits are automatically streamed from/to the PC. The SPI Xpress master can run single accesses or multiple queued accesses, **with no latency time between the accesses**. When queuing the accesses, it is also possible to use a special script command to insert idle times between the accesses, counted in number of clock cycles.

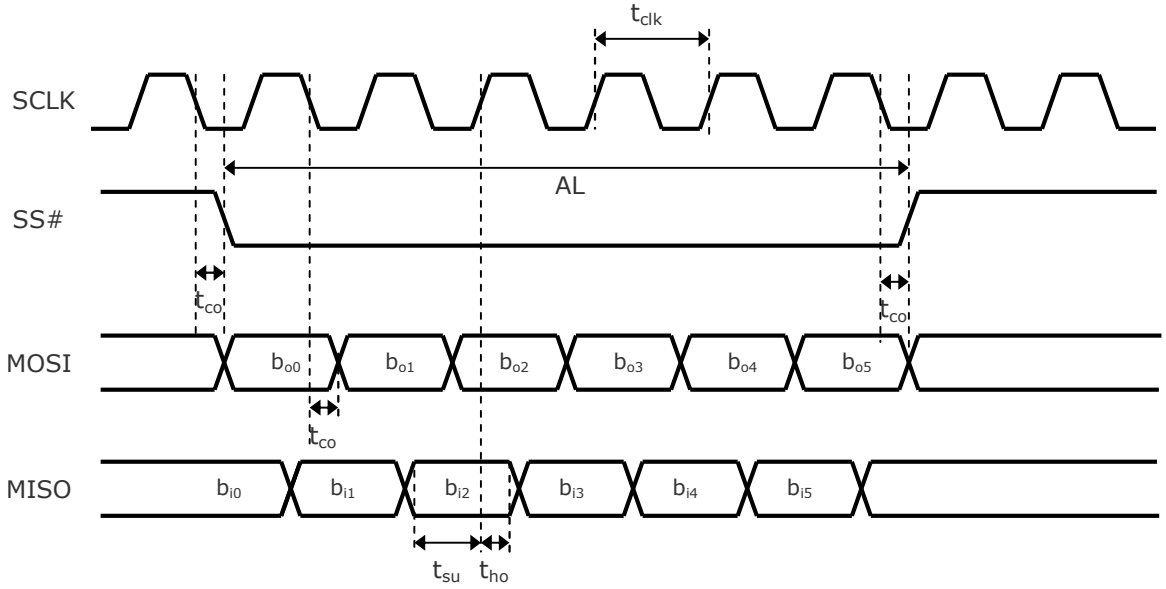

Figure 3 : Typical SPI access

Symbol	*Parameter*	*Min*	*Max*	*Units*
t_{clk}	Clock period	20	1,250,000	ns
t_{co}	Clock to output	0	4	ns
t_{su}	Setup time	5.6	-	ns
t_{ho}	Hold time	-	0.0	ns
AL	Access length	1	32,000 [1]	bits

Table 2 : SPI timing parameters

[1] Maximum access length is 32,000 bit if no SS shift option is selected. If SS edges are shift by ½ and ¼ TSCLK, then max. AL is 16,000 and 8,000 respectively.

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Flexible clock and control signals generation

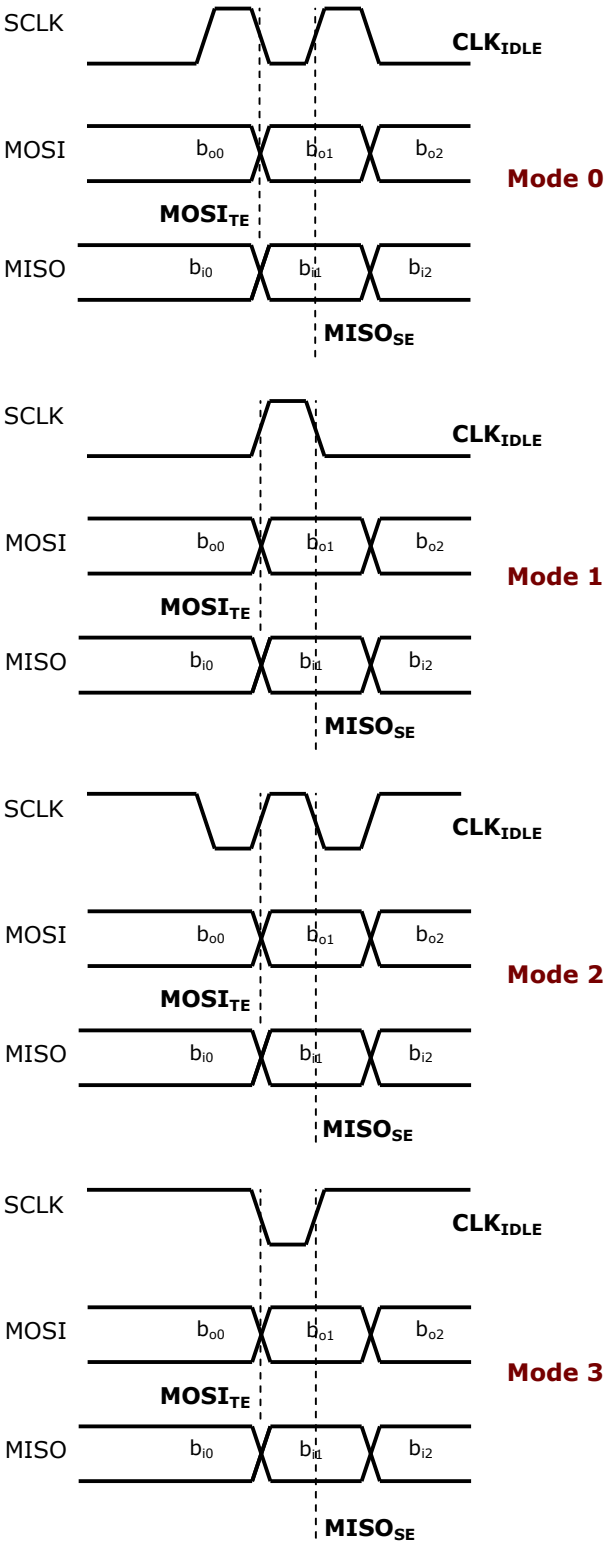
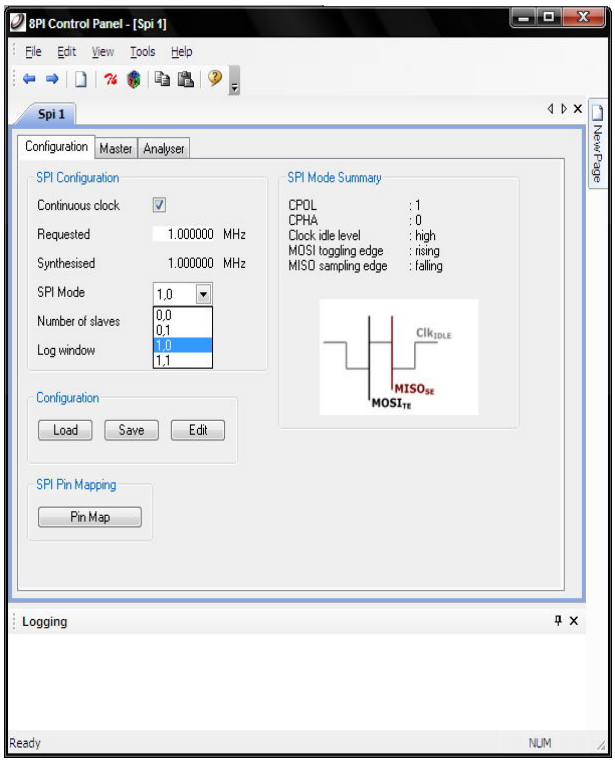


Figure 4 : SPI Xpress modes



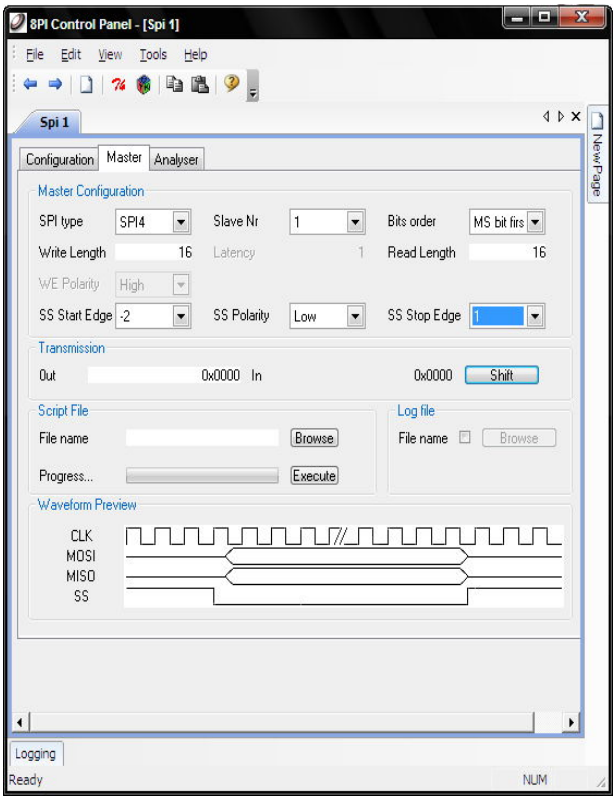


Figure 5 : SPI Xpress configuration and master tabs

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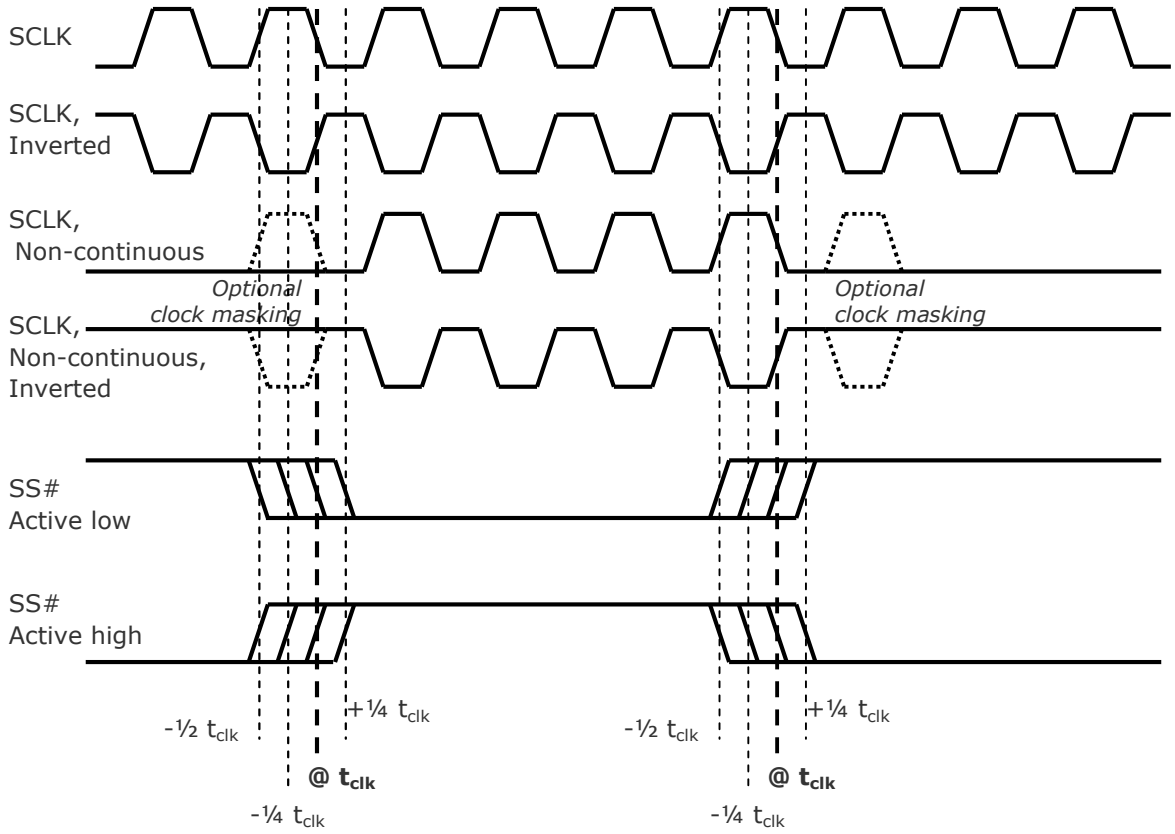

Figure 6 : SPI Xpress Master SCLK and SS# generation options

To be able to control a wide range of 4-wires serial protocols that derive from the standard SPI protocol, SPI Xpress master offers rich clock generation and control signal positioning options.

The SPI clock characteristics such as the frequency, the phase and the polarity are simply selected through the configuration tab of the SPI control application (refer to Figure 5).

Additionally, the SCLK signal can be generated as a continuous clock or an interrupted clock. In the latter case, the clock signal is generated only when data are sent / collected from the MOSI/MISO lines (refer to Figure 6).

SPI Xpress master also offers several other clock masking options at the SS# signals boundaries, as depicted on Figure 6.

Finally, the SS# (slave select) signals edges can be precisely positioned at or between the SCLK edges, with a resolution of ¼ of the SCLK period[2].

[2] SCLK frequency is limited to 25 MHz when using a phase shift of ½ TSCLK ;
SCLK frequency is limited to 12.5 MHz when using a phase shift of ¼ TSCLK.

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Extend control to 3-wires serial protocols

SPI Xpress is configurable into a 3-wires protocol master. In such case, SCLK and SS# are used together with a 'merged' MOSI/MISO line. Each transaction is a sequence of 3 length-configurable parts:

1. MOSI write: the SPI Xpress master writes a programmable number of bits onto the MOSI/MISO line;
2. Write-to-Read latency: to allow switching the direction of the access, the SPI Xpress holds the MOSI/MISO line in high impedant state during a programmable number of clock cycles;
3. MISO read: the SPI Xpress master samples a programmable number of bits from the MOSI/MISO line.

The clock polarity and phase options (CPOL / CPHA) are similar to these of the 4-wires protocols.
An optional WE output line provides the direction of the MOSI/MISO line, in case it is externally required.

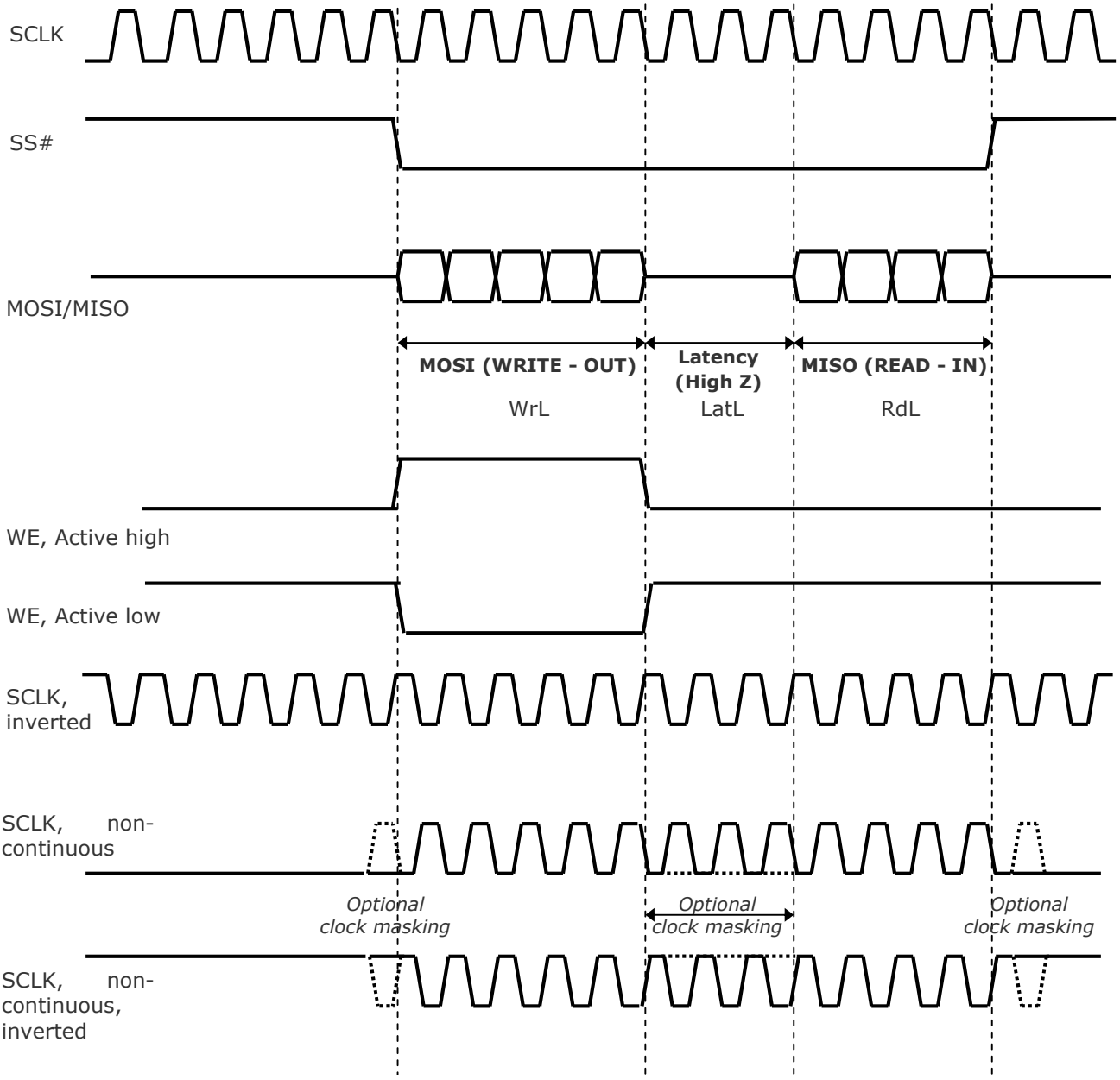

Figure 7 : SPI Xpress 3 wires protocols overview & clock options

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Symbol	*Parameter*	*Min*	*Max*	*Units*
WrL	Write length	1	4,095 [3]	bits
LatL	Write to Read latency length	0	400	bits
RdL	Read length	0	4,095	bits

Table 3 : 3 wires interface parameters

SPI Analyzer protocol interfaces

SPI Xpress is also a powerful SPI protocol Analyzer. Basically, it works like a logic analyzer; as for a logic analyzer, the following parameters are defined with the control software:

- Sampling rate;
- Start type: triggered or non-triggered;
- Edge or level trigger, pattern defined on up to 6 bits;
- Trigger positioning within the overall sampling window.

SPI Xpress Analyzer embeds GTK Wave waveform viewer, to get a direct view of the sampled data. By default, SPI Xpress Analyzer outputs the sampled data as **decoded SPI transactions**. These transactions can be **exported to a file and replayed into the SPI Xpress Master.** Additionally, the sampled data can be exported as raw data (samples) or raw SPI data, that is to say the samples located at the SCLK edges.

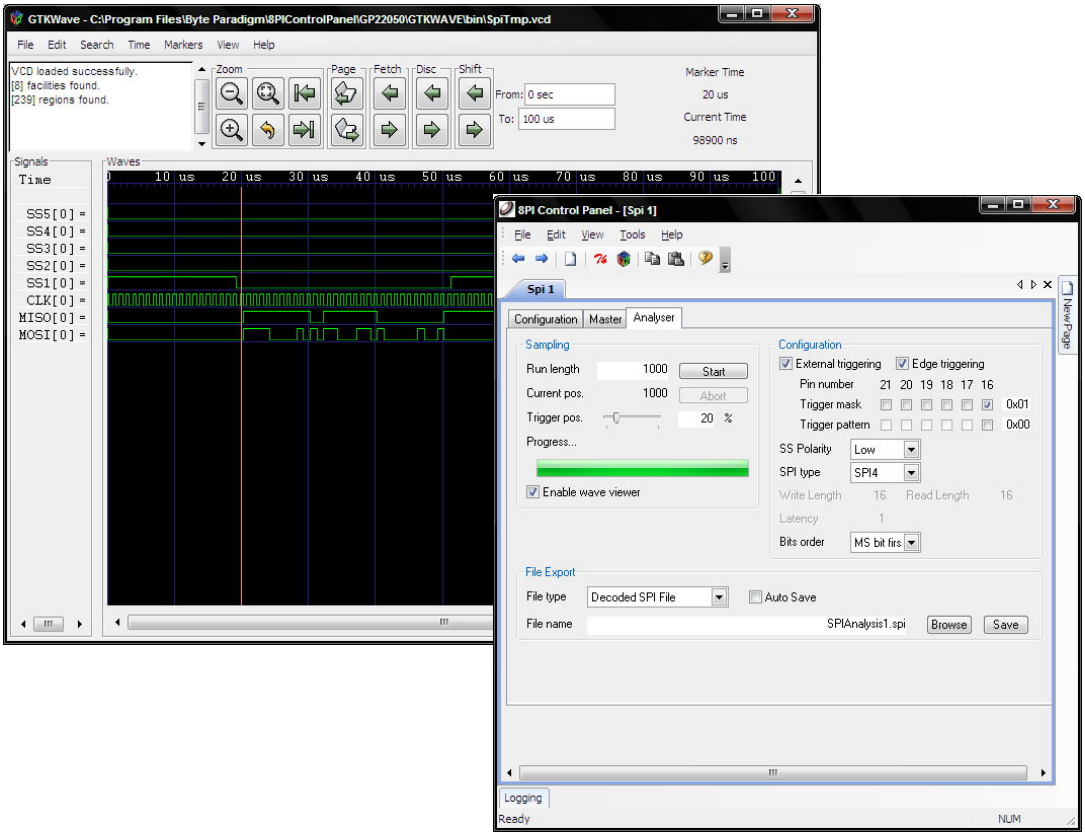

Figure 8 : SPI Xpress Analyser tab and waveform display

[3] The specified value is defined for accesses where SS edges are not shifted. Shifting SS edges by ½ or ¼ of TSCLK leads to max access length of 2,047 bits and 1,023 bits respectively. This is the case for WrL and RdL parameters.

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CLK	MOSI	MISO	Slave 0	Slave 1	Slave 2	Slave 3	Slave 4
1	1	0	1	1	1	1	1
1	1	0	1	1	1	1	1
0	0	0	1	1	1	1	1
0	0	0	1	0	1	1	1
0	1	0	1	0	1	1	1
1	0	0	1	0	1	1	1
1	1	0	1	0	1	1	1
0	1	0	1	0	1	1	1
0	1	0	1	0	1	1	1
0	1	0	1	0	1	1	1
1	0	0	1	0	1	1	1
1	0	0	1	1	1	1	1
0	0	0	1	1	1	1	1
0	0	0	1	1	1	1	1

Figure 9 : Example of SPI data exported as raw data

CLK	MOSI	MISO	Slave 0	Slave 1	Slave 2	Slave 3	Slave 4
0	0	0	1	1	1	1	1
0	0	0	1	1	1	1	1
0	0	0	1	1	1	1	1
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
0	1	1	0	1	1	1	1
0	0	1	0	1	1	1	1
0	1	0	0	1	1	1	1
0	1	0	0	1	1	1	1
0	0	1	0	1	1	1	1
0	0	1	0	1	1	1	1
0	0	1	0	1	1	1	1
0	1	1	0	1	1	1	1
0	0	0	0	1	1	1	1
0	0	1	0	1	1	1	1
0	1	0	0	1	1	1	1
0	0	1	0	1	1	1	1
0	0	0	0	1	1	1	1
0	0	1	0	1	1	1	1
0	0	0	1	1	1	1	1

Figure 10: Example of SPI data exported as raw SPI (sampled at the SCLK edge)

```
@idle 20
@shift4 2 16 0x1234 0xabcd
@shift4 2 16 0x5678 0x1dea
@shift4 2 16 0x9abc 0xabcd
@idle 100
@shift4 2 16 0x5a5a 0xffff
```

Figure 11: Example of decoded SPI data file

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